WORLD INTELLECTUAL PROPERTY ORGANIZATION
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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : G06K 7/10, G06F 15/24

A1

(11) International Publication Number: WO 92/15073

(43) International Publication Date: 3 September 1992 (03.09.92)

(21) International Application Number: PCT/US92/01461

(22) International Filing Date: 25 February 1992 (25.02.92)

(30) Priority data:
660,615 25 February 1991 (25.02.91) US
Not furnished 12 February 1992 (12.02.92) US

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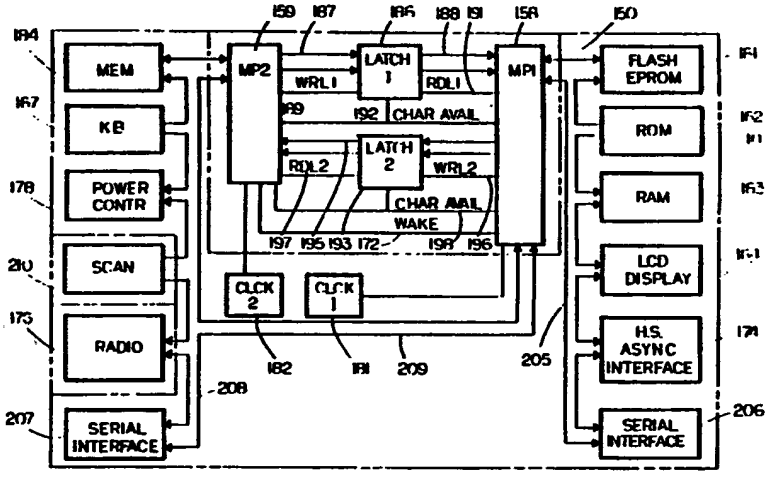
(81) Designated States: AT (European patent), AU, BE (European patent), BR, CA, CH (European patent), DE (European patent), DK (European patent), ES, ES (European patent), FR (European patent), GB, GB (European patent), GR (European patent), IT (European patent), JP, LU (European patent), MC (European patent), NL (European patent), SE (European patent).

Published
With international search report.

(54) Title: HAND-HELD DATA CAPTURE SYSTEM WITH INTERCHANGEABLE MODULES AND INTERACTIVE CONTROL CIRCUITS



(57) Abstract

A battery powered, portable, hand-held data terminal (10) of modular structure includes a base module (16, 136) with a keyboard (18) and a display screen (19) and their respective electrical functions (167, 164). A data and communications module may be selected from a number of different data and communications modules (48, 55, 75, 135) each having different types of data communications transceiver, or including in addition data collection devices, such as shelf label readers or bar code readers (76). The base module (16, 136) includes a microprocessor-controlled data communications and control interface having a predetermined protocol. To adapt the various type of data and communications modules for selection of any one thereof to become attached to the base module and function therewith, each of the data and communications modules includes a microprocessor (125, 144) operable to function as an emulator to interact with the microprocessor of the base module (16, 136).

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HAND-HELD DATA CAPTURE SYSTEM WITH INTERCHANGEABLE MODULES AND INTERACTIVE CONTROL CIRCUITS

Technical Field

This invention relates generally to data collection and processing systems using portable, hand-held data terminals for collecting, selectively processing and for communicating collected data to other system elements, and more particularly to control circuits which affect the operation of the data collection terminals.

Background of the Invention

Typical operations range from manually controlled processes to automated collection processes. Manually controlled collection processes may include reading data and manually keying in such read data. Typical automated processes may include scanning indicia of information with a scanner, for example a bar code reader. Data collected by such terminals may become part of the data base of the system. Real time use of data collected by the data terminals may be implemented by communication interfaces within such data terminals.

Though host computers functioning as central processing stations of such data systems may control data bases and data flow, the hand-held data terminals are key elements for operating the data systems efficiently. Current data systems using hand-held data terminals have shown a correlation between the functionality of the hand-held data terminals and the overall effectiveness of the systems.

While progress has already been made in improving efficiency and functionality of hand-held data terminals,

there is nevertheless a continued need for improving hand-held data terminals which are readily adaptable to perform various functions and communicate with a variety of communications equipment.

Summary of the Invention

According to a major aspect of this invention, one of a plurality of special purpose data and communications modules is selectively combined with a base module or unit of a hand-held data terminal unit.

According to one particular aspect of the invention, a base unit of a data terminal unit or data terminal includes a power-saving control circuit which includes first and second microprocessor elements or microprocessors. The first microprocessor which operates at a first clocking speed and consumes power at a first power level processes data. The second microprocessor which operates at a second clocking speed and consumes power at a second power level lower than the first power consumption level controls a selective operation of the first microprocessor. The first microprocessor is selectively deactivated after each data processing operation and the second microprocessor reactivates the first microprocessor on the occurrence of an event which requires data processing operations.

According to preferred features, a user interface is disposed in an upward directed surface which would typically be facing toward a person using the data terminal. The user interface typically features a keyboard adjacent a bottom end, and a liquid crystal display adjacent a top end of a substantially rectangular, elongate housing of the data terminal. The base unit provides for a data and communications module to be attached beneath the user interface and adjacent the top end of the housing.

According to another particular aspect of the invention, the data and communications module attachable to the base module includes a communications means of one

type, such as a radio using spread spectrum modulation transmissions, the data and communications module including provisions emulating data communications of a second type, the second type of communications and the respective protocol being compatible with data circuits of the base module.

According to a further aspect of the invention, the data and communications module to be attached to the base module may include provisions for data communications and a data scanner provision for collecting data.

In yet another aspect of the invention the data and communications module may include a modem and typical telephone communications coupling either in lieu of a radio communications provision or in addition thereto. The modem may be provided in the data and communications module with a data scanning device or with alternate data identification and collection provisions.

In one particular implementation including certain features of the invention, the data and communications module is contemplated to include the combination of a radio frequency communications provision and a data identification and collection provision, and an antenna of radio frequency communications provision of the data and communications module may be pivotally mounted to be pivoted to a position out of interfering relationship with the data identification and collection provision, while optimally receiving radio frequency communication.

In furtherance of efficient adaptability of data communications modules to base modules of the data terminals in accordance with the invention, it is contemplated to provide an elastic hand strap on the downward facing surface of a data terminal for retaining manual engagement with the data terminal, the hand strap being attached at one end thereof to a base module of the data terminal. A second, opposite end of the elastic strap is slidably inserted into engagement with a guide track disposed in an outer surface of the data and

communications module. The direction of insertion is in the direction of the one end of the elastic hand strap, such that an elastic tension in the hand strap retains the slidable engagement of the other elastic hand strap with the data and communications module of the data terminal. In accordance with the invention, the elastic strap is readily removed without tools by sliding the second end along the guide track in a direction against the tension of the elastic strap.

In a further embodiment according to the invention, in which a base unit includes a data and control interface for interacting with a data and communications module, an improvement in each of a plurality of data and communications modules includes a data and control interface provision including data and control signal conversion provisions for communicating data between the data and communication module and the base module in accordance with a data protocol resident within the base unit.

Various other features and advantages of the data terminal in accordance with the invention will become apparent from the following detailed description, which may be best understood when read with reference to the appended drawings.

Brief Description of the Drawings

FIG. 1 shows a frontal view of a modular data terminal and showing a frontal or upward directed face of the data terminal, as it would typically face an operator of the data terminal;

FIG. 2 is a side view of the data terminal shown in FIG. 1;

FIG. 3 is a side view of an alternate data terminal in accordance with the invention, a particular provision in accordance with certain features of the invention for engaging and disengaging a data and communications module with respect to a base module being illustrated;

FIG. 4 is a side view of an alternate data terminal

in accordance with the invention showing particular features relating to a data and communications module in combination with a base module, such features relating to the data and communications module having an RF communications provision and a data scanning provision and including further a pivotal antenna, all in accordance with the invention;

FIG. 5 is an exploded view of a pivot joint of an antenna in accordance with a particular aspect of the present invention;

FIG. 6 is a sectional view of the antenna pivot joint shown in FIG. 5;

FIG. 7 is a partial pictorial view of an upper portion of a data terminal in accordance with the invention, showing in particular a data and communications module having telephone connector plugs for interfacing the data and communications module with telephone communications lines;

FIG. 8 is a schematic diagram of functional blocks for illustrating contemplated major functional elements of a base module and a respective data and communications module of a data terminal in accordance with the invention;

FIG. 9 is a schematic diagram of functional blocks for illustrating the major functional elements shown in FIG. 8 and for illustrating the function of emulating the interface function required by an interface circuit communicating between non-compatible communications functions of the communications or data collection functions of the data and communications module and the base module;

FIG. 10 is a schematic diagram of functional blocks representing a particular embodiment of the invention showing a spread spectrum radio communication module interacting with the base module which is modified and includes a preferred power saving microprocessor circuit;

FIG. 11 is a schematic diagram of major functional

elements and their interaction of a particular embodiment of the base module including the power saving microprocessor circuit in accordance with the invention;

FIG. 12 is a schematic diagram showing typical, frequency related current characteristics of a first microprocessor element of the circuit shown in FIG. 11;

FIG. 13 is a schematic diagram showing frequency related current characteristics of a second microprocessor element of the circuit shown in FIG. 11;

FIG. 14 is a schematic block diagram showing functions allocated to each of the microprocessor elements or devices shown in FIG. 11; and

FIG. 15 is a flow diagram showing a desired functional interaction of the two microprocessor devices in FIG. 11 in accordance with the invention.

Detailed Description of the Invention

Referring now to FIGS. 1 and 2, a data collection terminal unit, also referred to herein as data terminal, is designated generally by the numeral 10. As shown in FIG. 1, a frontal face 12 of an elongate housing 14 of a base module 16 of the data terminal 10 typical faces upward and is accessible to the user of the data terminal. The upward facing portion of the module 16 houses a keyboard module 17, including an alphanumerical keyboard 18 and a display screen 19. The display screen 19 is in a preferred embodiment described herein a 4-line by 16-character Reflective Super Twist Liquid Crystal Display (LCD). Of course, other display means may be used in its stead. The keyboard 18 includes a lower, standard numerical keyboard section 21, above which is disposed an alphabetical keyboard arrangement 22. An On-Off power key 23 is preferably placed in a leftmost position of an uppermost row on an uppermost row of five keys. The outermost keys 24 in a bottom row are configured as "CLEAR" and "ENTER", while the remaining four keys in the uppermost row are preferably configured as a set of four user-defined function keys 26.

At a bottom end 30 of the housing 14, there are located two connector plugs 31 and 32 in recesses 33 and 34, respectively. Inasmuch as the connectors 31 and 32 are disposed in the recesses, adjacent end and interleaved protrusions 36 of the housing 14 extend somewhat past the connectors to protect the connectors from damage should the data terminal accidentally be dropped or set down on the bottom end 30. A preferred embodiment of the data terminal 10 is intended to withstand without damage a drop of about 1.2 meters to a solid surface, such as concrete. The preferred connector 31 is an input-output port, as may be used for such data collection as bar code reading, for example. In such instance, the connector 31 is preferred to be a 9-pin D-subminiature connector with pins interfacing to typical 5 volt scanning peripherals. The connector 32 may be used for accessing external power sources or provide of combined power and data communication. A circular miniature DIN-type connector 32 may be used in the preferred embodiment. A top end 40 of the preferred embodiment of the base module 16 typically may not include connectors. An antenna 41 shown to extend above the top end 40 is further described in reference to FIG. 2.

FIG. 2 is a side view of a data terminal 10 of FIG. 1. The base module 16 of the data terminal 10 includes an elongate upper housing portion 43 and a battery compartment 44 attached to the upper housing portion 43 adjacent the bottom end 30. In the preferred embodiment, the battery compartment 44 is assembled as a lower housing portion to the upper housing portion 43 and is equipped with a battery compartment door 46 which may be locked to seal an opening of the battery compartment 44. Adjacent the top end 40 of the data terminal 10 a data and communications module 48 is attached to the lower edge of the upper housing portion 43. The antenna 41 extends upward from the data and communications module 48 above the top end 40 of the data terminal 10. An elastic

hand strap 49 is attached to the underside of the data terminal 10. A belt clip 50 may conveniently be mounted to the hand strap 49, allowing the data terminal to be carried on a user's belt. The elastic hand strap is attached adjacent the top end of the data terminal to the underside of the data and communications module 48 and adjacent the bottom end 30 to a sloped lower surface of the battery compartment 46.

One of the features of hand-held data terminals as disclosed herein and in the PCT application PCT/US90/03282 incorporated herein by reference relates to the exchangeability of modules of different shape and varied function. The data and communications module 48 in FIG. 2 may for example include a radio module which is externally identified by the antenna 41. The radio module may be a commercially available pretuned 1-watt (UHF) frequency modulated (FM) radio transceiver module, or any similar radio module, such as a Motorola P10™ radio model, for example.

In accordance herewith it is contemplated to provide the data and communications module 48 as a module which is readily replaceable with another data and communications module. Each such module will feature a quick exchange mounting mechanism, such as is more clearly illustrated with respect to FIG. 3, and any of a number of features packaged in one of a number of compatible data and communications modules. When mounted, the module, such as the data and communications module 48 is matched in a contour continuation along a juncture 52 to the adjacent edge of the battery compartment 44 and along a longitudinal parting line 53 of the base module 16. For example, the data and communications module 48 is sized to include the described radio frequency transceiver module, as indicated by the antenna 41. Other data and communications modules may include a similar radio frequency transceiver module and may include additional memory capacity to function with the base module 16.

Various combinations of features are contemplated in accordance herewith.

FIG. 3 shows the base module 16 and substantially in a ready position to become mounted to the base module 16 is a data and communications module designated generally by the numeral 55. The data and communications module 55 is shown to represent generally a number of such data and communications modules which may be desirably incorporated into a communications system in accordance with the invention. It may be noted that the data and communications module 55 is shown in FIG. 3 as being of somewhat relatively greater depth or thickness than the data and communications module 48 described with respect to FIG. 2. The change in outer dimensions illustrates that a number of modules of various depth are adapted to match with mounting provisions to attach the respective data and communications module 55 to the base module 16.

The data and communications module 55, as a representative module featuring the attachment to the base module 16 has a plurality of laterally disposed latching hooks or latch hooks 56 which become engaged by respective latching seats or latch seats 57 disposed along the adjacent edge of the base module 16 when the module 55 is moved toward and into engagement with the adjacent edge and then toward the battery compartment 44, as shown by the arrow. Electrical communication is established via a power and communications connector 61 the pins of which engage a mating connector socket 62 within the base module 16. A set of screws 63 may be tightened through the battery compartment 44 into a set of threaded seats 64 disposed in the adjacent wall of the module 55 to securely retain the attached module as an integrated part of the data terminal 10. At the top end of the data terminal 10, a lip or extending stop edge 66 of the module 55 engages a complementarily shaped seat 67 at the top end of the base module 16 to securely interlock the data and communications module 55 with the base module 16.

It is contemplated, for example, for the module 55 to include any of a number of combinations of diverse functional elements. For example, the module 55 may include the aforementioned transceiver, though the antenna 41 may be attached externally as shown in FIG. 2 or might be provided internally, in addition to extended data memory capacity, a modem or a reader of indicia of information may be included, such as a bar code reader, or a shelf tag reader. Shelf tag systems are known in which so-called "shelf tags" contain means for programming information into small display devices which are attached to front edges of merchandise storage shelves. The devices or tags would then retain the programmed data which may be acquired by the reader in the data and communication module 55, for example. Information may be communicated between the shelf tag and the data terminal 10 by various means including radio frequency or optical transmission. Information may be communicated via optical readers in the data and communications terminal 16 as read from liquid crystals, or by other communication such as infra red optical, or low power RF data messages.

FIG. 4 shows an alternate embodiment of the data terminal 10 in which the data terminal includes a data and communications module which includes, for example, a radio frequency transceiver module 75 and a CCD scanner module which may be disposed in a lower portion of the module 75 at 76, having a scanning window at 77. Since it may be desirable to position the scanning window near a surface at which data indicia such as bar code labels may be located, as indicated at 78, the antenna which also protrudes from the top end of the data terminal 10 is found to be interfering when disposed in a normally protruding position. It is therefore contemplated to arrange the antenna 41 in a manner in which it may be pivoted from an upwardly protruding position, such as shown in phantom lines at 81 to a tilted position such as shown by the antenna 41.

In reference to FIGS. 5 and 6, there is shown a pivotal joint which experiences little signal degradation when pivoted from such upwardly extended position to the tilted position in which the scanner window may be brought into proximity of a bar code label, for example, as described. The pivotal antenna joint includes a pivot base or pivot socket 83 into a hollow cup of which fits a pivot ball 84. Both the pivot socket 83 and the pivot ball 84 are of RF dielectric to prevent radio frequency burns of a person touching the antenna when the associated radio transceiver is transmitting. The pivot socket 83 is mounted against an outer wall of the module, such as the module 48, 55 or 75 by an antenna swivel post 85. The swivel post 85 includes a spherical top against which rests a pivot washer 86. The pivot washer is in turn urged into contact with the top of the swivel post by a cupped spring washer 87, also at times referred to as Belville washer. The urging force against the spring washer 87 is provided by a doubly-threaded antenna mounting bushing 88. An external thread of the bushing 88 screws into an upper opening of the pivot ball 84 to complete the pivot joint of the antenna. The antenna 41 screws with its base into the internal threads of the mounting bushing 88. As shown in FIG. 6, a lower dielectric skirt 89 of the antenna 41 extends downward over the outer edge of the bushing, which is of metal, to prevent exposure of the bushing. It should be understood that variations in the pivot joint may be possible within the scope of the invention.

FIG. 7 shows another embodiment and further features of the invention as described herein. The elastic strap 49 may be permanently attached adjacent the bottom end of the data terminal 10 as described herein above. At an upper end, however, the elastic strap may be attached to the exchangeable data and communications modules, such as a module 90 depicted in FIG. 7. In that the modules are exchangeable and in an effort to facilitate a quick

replacement of one module for another, the hand strap is attached to the module 90 by a guide structure 91 including left and right hand spaced guide tracks 92 and 93 which receive a guide bracket 94 attached to the upper end of the hand strap 49. To attach the upper end of the hand strap 49 the elastic hand strap is stretched beyond its normal tensioned stretched length and the guide bracket 94 is inserted into an uppermost opening between the guide tracks 92 and 93. The tension of the hand strap 49 pulls the bracket 94 into the space between the guide tracks 92 and 93 in the direction of the arrow 95. The insertion of the bracket 94 securely captures the strap 49 at its upper end. To remove the hand strap at its upper point of attachment, the bracket is simply pulled out of the uppermost opening between the two spaced guide tracks 92 and 93. The embodiment of the data and communications module 90 further shows typical telephone connector jacks 97 and 98 indicating that the module contains a typical modem unit for communication over standard telephone lines. The modem unit as shown by connectors 97, 98 in the module 90 may be supplemented by memory for data storage prior to communication by the modem. In this manner the data terminal may be used in a batch process mode, data being transmitted at times and occasions convenient for telephone hook-up. Modem connections may also take on more significance in that the data terminal may be coupled to a typical cellular telephone unit which in turn can communicate via standard telephone communication networks over vast areas. In the latter mode batch transfer of data may still be desirable, though the need for substantial data storage capacity may be reduced.

FIGS. 8 and 9 illustrate a microprocessor controlled data transfer between the base module 16 and any of a number of data and communication modules which may include various data collection and data communication transceivers including complex radios such as a spread

spectrum radio or such a modem for telephone transmission of data. Though not expressly described, it is understood that the hand-held data terminal 10 as described herein and all of its circuits, including those of attached modules are powered by a battery or power source which occupies the space of the battery compartment 44 as described herein. FIG. 8 shows a block diagram of functions of the base module 16 and a typical data and communications module designated generally by the numeral 100. The base module is operative in conjunction with a typical radio frequency transceiver provided by the data and communication module 100, for example. The base module 16 includes a typical keyboard module 102 interactively coupled to a microprocessor 104. A preferred microprocessor is a 80C196KC device which is a 16-bit microcontroller 105 with on-chip masked ROM, RAM and built-in timers, ports, analog to digital converters and a serial interface 106. Thus, the microprocessor functions as a microcontroller and as an interface for communicating data and control signals to and from the base module 16. In addition to the on-chip memory capacity, an external ROM 107 and an external RAM may be provided for additional data processing and communication capacity. Display controller and driver circuits 109 may be multi-chip circuits or may be integrated into a single device to drive the described LCD screen 110. The driver circuit is controlled by the microprocessor 104 either by direct link or via a general data bus, such as data bus 111. A typical scanner interface 115 is coupled to a 9-pin connector 116, such as the referred to D-subminiature connector which may couple a laser scanner or CCD scanner to the base module 16 for data collection.

The data and communication module 100 is of particular interest in that an improved interfacing may be obtained by coupling communication between the data and communication module 100 and the base module 16 through a microprocessor 125, such as, for example an 80C51

microprocessor circuit. Typical on board ROM allows the microprocessor to be programmed to interact with a number of devices in accordance with the stored program. The microprocessor interacts with an interface circuit 126 which may be an analog or mixed analog and digital interface circuit. The program for interacting with the interface circuit 126 may also be stored within a ROM of the interface circuit 126. The interface circuit 126 is coupled to a transceiver module 128. The microprocessor 125 may also be coupled directly to a data collection interface 129 to receive data from a scanner for reading any number of different bar codes or for providing input data from other external sources. The operation of the microprocessor 125 for coupling data to the base module 16 allows various input patterns to be processed by any of specific operational protocols controlled by the microprocessor 125, such that the data input from the data collection circuit can be made the same from any of a number of devices. Also with respect to the operation of the transceiver, in that the program for operating the microprocessor 125 may include particular address codes for data retrieval and data communication via the transceiver, the data sent via a data and control bus between the microprocessors 125 and 104 can emulate a uniform data transfer protocol to the base module 16. The simplification resulting from the microprocessor 125 increases the number of communications devices that may be represented by the data communication transceiver circuit or module.

Referring now to FIG. 9, the base module 16 is shown as being coupled to a different data and communications module designated generally by the numeral 130 in which the interface circuit 126 shown in FIG. 8 has been replaced with an interface circuit 132 and the transceiver 128 in FIG. 8 has been replaced by a transceiver circuit 134. The transceiver 134 may for example be a complex radio, such as a spread spectrum radio in lieu of an FM

transceiver, as represented, for example, by the block identified at 128 in FIG. 8. However, the program function represented by the interface circuit 132 and interacting with the microprocessor 125 permits the interactive control and data stream between the base module 16 and the data and communication module 130 to be emulated to appear to the base module 16 as being the same as the simple FM transceiver module. The reference to the particular microprocessor circuit types in the base module and in the base module 16 and in the communication module 100 or 130 are given as illustrative examples and should not be considered as limiting to the scope of the invention. The data collection interface 129 is considered optional and may not form part of the communication modules 100 or 130 when the communication module does not include a scanner module, such as indicated at 76 in FIG. 4. In either case the microprocessors 104 and 125 interact, each controlling the environment of its respective submodule, such as the base module 16 or the data and communication module 130, to enhance data exchange between the modules.

FIG. 10 shows a communication module 135 communicatively coupled to a base module 136. The base module 136 may be structurally similar or identical to the described base module 16, the electrical control functions and circuits include certain power saving functions and circuits as further described with respect to FIGS. 10 through 15. The communication module 135 is a preferred spread spectrum radio module. Spread spectrum radio transmission and receiver functions are shown with a symbolic antenna 137 as a single transceiver 138 ("SS RADIO"). Spread spectrum radio technology is well known in the art as permitting high binary data rate transmissions which are propagated over a selected channel frequency within an assigned 902 to 928 Mhz commercial frequency band. Spread spectrum communication may use a pseudo-noise encoding mechanism according to which data

are encoded, transmitted, received and decoded at respective transmitting and receiving stations. Both the transmitting and the receiving station must of course employ identical encoding and decoding algorithms. The encoding and decoding function is shown as a spread spectrum radio modem circuit 139 ("SST"), an integrated circuit device which might well be considered an integral element of the spread spectrum radio unit. Spread spectrum radio transmissions are capable of encoding, decoding and transmitting binary data messages at relatively high rates in comparison to other data transmission rates. While state of the art facsimile transmissions and typical FM radio transmissions may take place at signalling rates of 9600 baud or bits per second, in a preferred embodiment a spread spectrum binary transmission rate is 192 thousand bits per second. A transmitted message includes of course besides data bits various control and error checking bits. Outgoing messages are modulated and incoming messages are demodulated by the modem circuit 139 and are communicated as synchronous demodulated serial messages between the modem circuit 139 and a high level serial communication controller 141 ("HSCC"). A timing function circuit 142 ("TIMER") is shown as being coupled to the communication controller 141. It is to be understood, however, that the timer 142 is also functionally coupled to the circuit 139 and further provides timing signals to operate a radio module microprocessor circuit 144 ("PROC CRCT.") and an associated external memory circuit 145 ("DAT MEM").

The serial communication controller 141 performs control functions on data messages, such as error detection and correction, and converts data messages from synchronous serial to parallel binary data. The controller operates under a known communication protocol referred to a High level Data Link Control or HDLC. Data are communicated between the serial communication controller 141 and the microprocessor circuit 144 in a

synchronous parallel data format. The microprocessor circuit 144 receives and temporarily stores received data in a typical memory circuit represented by memory circuit 145. Data are then communicated by the microprocessor 144 as high speed asynchronous data communication messages between the communication module 135 and the base module 136. The microprocessor 144 is preferably an H8 type microprocessor which includes on-board memory in the form of both ROM and RAM circuits. The on-board memory stores the communication control instructions by which the microprocessor 144 communicates with the respective data circuits in the base module 136. However, to adequately support temporary storage of data messages to relay them as either synchronous or asynchronous communication messages between the modules 135 and 136, the memory circuit 145 externally of and in addition to the on-board memory is available to the microprocessor 144.

The circuit functions in the base module 136 of FIG. 10 depict a power-conserving microprocessor control circuit 150 which includes a combination of two microprocessor elements 158 and 159. The microprocessor elements 158 and 159, individually capable of functioning independently of each other are coupled to interact as a functional control unit to conserve power when compared with a conventional microprocessor controlled circuit. The microprocessor 158 which is referred to as application processor 158 is applied to perform data processing and data manipulation operations of the data terminal 10. The second microprocessor 159 is referred to as a control processor 159. The application processor 158 operates faster than the control processor 159 but also consumes more power. However, to conserve power in the combined operation of the two processor elements 158 and 159, the application processor becomes deactivated after completion of any data processing task. Since data storage and screen display of data are memory intensive functions of the application processor 158, the processor 158 is

coupled to a full complement of memory including programmable read only memory 161 ("FLASH EPROM"), permanent memory 162 and random access memory 163 ("PSRAM"). Though the application processor 158 updates a screen display 164 ("LCD DISPLAY"), the control processor 159 controls a contrast adjustment 166 ("CONTRAST LCD DISPLAY"), the commands for which may be received from an operator through a keyboard 167 ("KB"). Data and control characters are communicated between the application and control processors 158 and 159 via an interface circuit 168 ("INTRFACE CRCT"). The interface circuit may be an integrated circuit which further includes functions for applying respective clocking signals from a clocking signal source 169 ("CLK1") to the microprocessors 158 and 159. The interface circuit also may include functions such as the control of an EL panel backlight drive 171 ("BCKLIGHT DRIVE").

Since the application processor 158 becomes deactivated upon completion of a data processing task, the control processor 159 functions to reactivate the application processor 158 upon occurrence of an event that necessitates data processing or manipulation. Such activation is preferably provided by a direct connection between the two processors 158 and 159 as shown at 172. High speed data transfer between the communication module 135 and the base module 136 of the data terminal 10 are preferred to take place directly between the microprocessor 144 of the communication module 135 and the application processor 158 via a high speed asynchronous communication interface circuit 174 ("HS ASYNC INTR FACE"). In a preferred data receiving operation the microprocessor 144 would prompt the control processor 159 to reactivate the application processor 158 to receive incoming data through the interface circuit 174. Reactivation of the application processor 158 for an outgoing message may be prompted by an operator from the keyboard 167.

Referring to FIG. 11, the schematic diagram shows major functional logic and communications elements of the power-conserving microprocessor circuit 150 which may be controlling the operations of, or be functional in the operation of, the hand-held, portable data terminal 10, schematically identified by encompassing box. The data terminal 10 may interact in particular with one or more temporarily attached or integrated peripheral communication devices or modules, such as a transceiver communication module ("RADIO"), shown at 176. The communication module may be a standard FM transceiver adapted for digital data communication, or it may be the spread spectrum communication module 135 described with respect to FIG. 10. The data terminal 10 of the described example being portable, the physical circuits of the functional devices shown in FIG. 11 typically would be powered by a battery 177 (shown schematically in FIG. 14) which is included in the power management function 178 ("POWER CONTR"). The microprocessor operated control circuit 150 comprises, as referred to with respect to FIG. 10, a combination of two circuit portions which include specifically the two microprocessor type subcircuits 158 and 159. Each of these subcircuits 158 or 159 are separately functioning microprocessor blocks, modules or separate microprocessor devices. In reference to FIG. 11 the devices are respectively the application processor 158 ("MP1") and the control processor 159 ("MP2"). It is advantageous to perform data processing operations at a comparatively high speed and with a more powerful processor than would be desirable for relatively less complex control functions.

The term "data processing operation" is used herein in the sense of manipulating a series of binary codes according to programmed instructions to arrive at a desired result. Because of the great number of discrete binary operations required to perform many of the most common data processing functions, higher processor speeds

and more complex or powerful microprocessor circuits of those typically available are more desirable for data processing operations.

A characteristic of more powerful microprocessor devices and those operating at higher speeds is that these devices also consume more power. However, in accordance herewith, the power consumption of a microprocessor circuit may be limited as further described. For example, in the preferred embodiment, the application processor or data processing processor device 158 is an "Intel 80C188EB" device which is "16-Bit" microprocessor device, operated at a preferred speed of 9.2 megahertz (MHz). At such preferred clocking speed of 9.2 MHz, the power consumption or operating current consumed by the data processing microprocessor device 158 is approximately 55 milliamps ("mA"). The control processor 159 is in a preferred implementation a "Hitachi H8/325" device which is an "8-Bit" microprocessor, operated at a preferred speed of one-half of the speed of the data processing microprocessor 158, or 4.6 MHz. Because of the smaller physical size of the control processor 159 and the slower, preferred clocking speed, the power consumption or current required by the control processor 159 in its operational mode is only about 9 mA, hence less than one-fifth of the power consumed by the processor 158. Because of continuous advances in the field of microprocessors over the past decade, it is to be expected that in the future other microprocessors will be marketed which will meet or exceed the requirements of the presently preferred microprocessors and that these microprocessors also may operate in accordance herewith. In general, the control microprocessor circuit or the control microprocessor 159 desirably operates at a slower and less power consuming speed than the application microprocessor circuit or the application microprocessor 158. A one-to-two speed ratio for driving the respective microprocessors 159 and 158 is preferably chosen because of the power savings that are

being realized with respect to the portable data terminal 10. Respective clocking circuits 181 and 182 ("CLCK 1 and CLCK 2") are shown as providing respective timing signal ports coupled to the respective processors 158 and 159 to drive the processors at the desired speeds as described.

Also, a functional arrangement of the separate clocking circuits 181 and 182 preferably may be replaced by the single crystal oscillator circuit 169 ("CLK 1") which is then coupled through the interface circuit 168 ("INTERFACE CRCT") to both processors 158 and 159 as shown in FIG. 14. The interface circuit 168 would include in such coupling arrangement a typical divide-by-two timing circuit function. An original 9.2 MHz clocking signal port and a signal port with the divided by two signal, comparable to the clocks or timing signal ports 181 and 182, would be coupled to the respective timing signal input ports of the processors 158 and 159, respectively, to drive the processors 158 and 159 at their respective speeds of 9.2 and 4.6 MHz. A second clock 183 ("CLK 2") shown in FIG. 14 may provide what is referred to as "real time" timing functions such as actual time and date information.

As will become apparent from the further description, it is within the scope of the invention to integrate the distinct functions and operational characteristics of the separately identified microprocessor devices 158 and 159 into a single integrated device. The resulting integrated device 150 desirably includes respective interface functions as are further described herein to implement the power-saving characteristics realized by the presently preferred embodiment of the control circuit 150. Within such integrated device 150, the function of the application processor 158 is then performed by a first microprocessor circuit block or circuit portion, and the function of the control processor 159 is performed by a second microprocessor circuit block or circuit portion. These circuit blocks, portions or modules interact

essentially in the same manner within the circuit 150 as the currently used microprocessor devices 158 and 159.

The preferred control processor 159 includes in its commercial implementation in addition to typical microprocessor registers and an arithmetic logic unit such functional circuit blocks as ROM, RAM and communications ports. These circuit blocks may also be included in any integrated device 150, or their functions may be supplied by peripheral devices. As shown in FIG. 11, additional external memory 184 ("MEM") may optionally be provided to supplement such on-board memory 185 ("OM"), though for typical operations as further described herein, the external memory device 184 is not required. According to a preferred embodiment, data communication between the processors 158 and 159 occurs via an interface circuit including, for example, two 8-bit data registers or latches described in greater detail with respect to the further description relating to FIG. 11. It is to be understood, however, that the control processor 159 may have a direct bus interface provision and become directly coupled to the application processor 158, the coupled processors 158 and 159 thereby being capable of bidirectionally passing data and control signals without the described two 8-bit data registers or latches. The interface circuit 168 shown in FIG. 14 should be understood to not only include the clocking signal coupling circuits to drive the respective application processor 158 and the control processor 159, but to further include the data interface or bus to permit the desired bidirectional data and control code communication between the processors 158 and 159 as further described herein. In further reference to FIG. 14, an integration of the processor devices 158 and 159 into a single device desirably may include the interface circuit 168 as an integral part of the integrated circuit 150.

Referring again to FIG. 11, a first latch 186 ("LATCH 1") of the two latches is coupled through an 8-line

parallel bus 187 to the microprocessor 159 and through a similar bus 188 to the microprocessor 158. Respective write and read lines 189 and 191 ("WRL1 and RDL2") provide respective control or trigger signals for the processor 159 to write data into the first latch 186 and for the processor 158 to read data from the latch 186. A handshake or control signal line 192 ("CHAR AVAIL 1") toggles between a high or "logical 1" to indicate to the processor 158 that data have been read into the first latch 186 by the processor 159 and a "logic 0" to signal that the processor has read or taken the data from the first latch 186. A second latch 193 ("LATCH 2") similarly stores an 8-bit data element written into the second latch 193 by the processor 158 over a second write 8-bit write bus 194. A second read bus 195 transfers the data element stored in the second latch 193 from the latch to the second processor 159. The control or trigger signals for writing into or reading from the second data latch 193 are provided over trigger lines 196 and 197 ("WRL2 and RDL2"), respectively. A second handshake or control signal line 198 ("CHAR AVAIL 2") coupled to the second latch 193 and to the processors 158 and 159 also toggles between high and low signal states to indicate in the high state the availability of data in the second latch 193 and in the low state the completion of a read operation of the most recent data element by the control processor 159.

The control signal line 172, referred to with respect to FIG. 10, carries a control signal generated by the control processor 159, by which the control processor 159 controls the duty cycle of the application processor 158. In reference to FIGS. 12 and 13, the current usage and respective power consumption of the control processor 159 ranges between a typical operating mode and a typical "idle mode" at the preferred frequency of 4.6 MHz between a high of 9 and a low of about 7 mA, as shown in FIG. 12 by graphs 201 and 202, respectively. It should be realized that even while considered "idle", the control

processor maintains power to internal memory and performs typical periodic monitoring functions, such as strobing the keyboard circuit 167 ("KB") for a "Depressed Key" signal, for example, or routinely monitoring the power management function 178, such as for a "Low Battery" indication. However, even when in the typical operational mode as indicated on the current vs. frequency graph 201, the control processor uses only about one-sixth of the current used by the application processor 158 in its preferred operational mode. On the other hand, when the application processor 158 is placed into an idle state in which the device 158 is not driven by a clocking signal, the idle state current requirement has a specified maximum rating of 0.1 mA, as shown by the high-low indicated values at the 9.2 MHz frequency mark at and below graph 203 in FIG. 13, in which graph 203 indicates the typical operating current consumption of the application processor 158. It is to be noted that a deactivation of the application processor 158 could be implemented by a complete electrical shut down of the device. However, because of the low non-clocked power or current draw of the application processor 158, the application processor function is preferably deactivated by eliminating its clocking signal but maintaining the device 158 under DC bias. Removing the clocking signal from the application processor function achieves a desired power-down idle state while permitting the device 158 to be reactivated momentarily by an appropriate "wake up" control signal from the control microprocessor 159.

Tests have shown that typical data processing operations performed by the application processor 158 require approximately 10 milliseconds of time and not more than 20 milliseconds on the average of all operations which are typically performed by the application processor 158. It has further been found that a more user friendly and a more practical response time may be obtained from the data terminal 10 and less power is required when

substantially all data processing operations are performed by the application processor 158 and the application processor is subsequently immediately deactivated, than if a single alternative microprocessor circuit were used which would operate at a higher rate and would include sufficient computing capacity to perform all required functions in good time. The combination of the application processor 158 and the control processor 159 amount in the preferred selection of the two processors only to an approximate increase in current usage of typically about ten percent and in the extreme of no more than 20 percent over the normal operating current level of the control processor by itself. An upper combined power consumption of the application processor 158 as controlled by the control processor 159 and the control processor 159 itself is about one fifth of the power consumption of the application processor when it is operated continuously. However, the display speed and data manipulation speed of the data terminal 10 essentially is the same as if the data terminal were controlled by the more powerful application processor 158.

The operating current requirement for the application processor 158 is related to the increased number of actively switching elements in each computational operation. Though having an interrupt function, the preferred 80C188EB processor 158 does not include, in contrast to the control processor 159, any internal memory devices. FIG. 11 consequently shows a data bus 205 of the processor 158 coupled to external memory devices, such as a flash electrically erasable and programmable read-only memory 161 ("FLASH EPROM"), a read-only memory 162 ("ROM") and a typical random access memory 163 ("RAM"). The data bus 205 further couples the application processor directly to the data display 164 ("LCD DISPLAY") of the data terminal 10, such as a dot addressable LCD graphic screen, for example. A direct data transfer by the high speed application processor 158 to the LCD screen is preferred

because of substantial amounts of data handling or processing that is required in updating a particular screen. For example, even a small graphic screen display, such as a preferred screen of 48X100 pixels, requires that each of the pixels be updated on a continuous basis. Typically control circuits, which are typically part of the data display function 164 and are not separately shown, and which may be specific to a particular screen display may routinely re-apply currently displayed information dots in a cyclic refresh operation to the already identified pixels of the screen. However, in any updating of the screen, such as a simple display line scrolling operation, which an operator may not even consider noticeable or significant, each pixel of the screen must be updated. To perform such updating of information in a power efficient manner, a data processing operation and the high speed passing of the updated data between the RAM memory 58 and the data display 164 is most power-economically and most promptly and, hence, most user-friendly performed by a short operational activation of the application processor 158. More data processing with respect to the data display screen 164 may be required for routine menu operations. Menu operations are particularly desirable for such portable data terminals 10, in that the typical user would not be expected to be well acquainted with computer terminals. Well defined menu operations with a number of available menu levels are found to significantly increase the usefulness of a data terminal unit. An efficient menu operation is known to involve data base searching and data retrieval in addition to the normal display screen updating operation. In the above-described operations the described microprocessor circuit with the selectively activated data processing device 158 and the relatively smaller and slower control processor 159 has been found to be particularly advantageous.

A selective activation and deactivation of the

microprocessor circuit portion implemented by the data processing device or application processor 158 would also provide for power savings when the operating speeds of the two processors 158 and 159 are the same. Though in the event of both processors 158 and 159 being operated at the same speed, the power savings do not appear to be as prevalent as realized in accordance with the preferred embodiment of the described invention.

A further function to be advantageously addressed by the application processor 158 is the data communication with the high speed asynchronous communication interface 174 ("H.S. ASYNC INTRFCE"), in support of facsimile or external display screen operations. Of less significance, yet typically power saving, are data communications to an RS-232/RS-485 serial interface 206 ("SERIAL INTERFACE"). However, it should be realized that certain communications operations, such as outgoing communications to a printer (not shown) for example, may also be communicated under the control of the control processor 159. Even when the application processor 158 selects data for communication to a line printer, a typical printer speed, except in a graphics mode would be sufficiently slow to allow the application processor 158 to operate in an intermittent, power saving mode. FIG. 11 consequently shows a second RS-232/RS-485 interface 207 ("SERIAL INTRFCE") coupled to a second data bus 208 which is further communicatively coupled to the control processor 159 to support the above described data communication operation via the control processor 159.

The data bus 208 is further shown as being coupled through a bus extension 209 directly to the application processor 158. The data bus extension 209 is particularly provided for direct data communication between the application processor and a data scanner 210 ("SCAN"), which may for example be a bar code reader. Because of the high rate at which data are generated by the operation of a data scanner, the data are most reliably received,

processed and stored by the application processor, though the operation may not be power saving as such. A scanning operation may consequently involve the operation of both the application processor 158 and the control processor 159. According to a preferred operation of the control circuit 150, the control processor 159 monitors the circuit function of the data scanner 210 to detect a control signal which indicates the event of a scanner trigger depression and that a scanning operation of an associated physical scanning device is about to begin. The scanning operation results in a string of data appearing at the data bus 208 and the associated data bus 209. Since the application processor 158 is likely to be idle at the time of the occurrence of a trigger signal, the control processor places a "wake-up" signal on the control signal line 172 to activate the application processor 158. The control processor 159 further writes an 8-bit control character into the first latch 186. Upon completion of loading the control character into the data latch 186, the control processor 159 places a "one" signal on the character available line 192 to allow the application processor to read the control character from the latch 186. The application processor reads and decodes the control character in accordance with protocol instructions read from the ROM memory 162, for example. In the example of a scanner trigger indication, the decoded control character would signal the forthcoming string of information to be received by the application processor 158 directly from the scanner 210 over the data bus 209. Hence in contrast to being conditioned for the event of receiving data from the keyboard 167 or from the radio 176 which data might preferably be received over the data latch 186, the application processor would in the event of scanned incoming data be conditioned to read the "event data" as a string of data directly from the data bus 209. The term "event data" is used to describe data relating to an event. Any time event data requires

processing, such event data would be routed to the application processor 158 either directly as described with respect to the scanner data or between the two processors 158 and 159, such as by the interface 168, for example. It is to be understood that conditioning the application processor to receive a string of data directly via the bus 209 need not be limited to the receipt of the scanner data but is contemplated with respect to any such future uses of the data terminal 10 which requires any high volume of data to be received and processed within a, comparatively to other typical serial receipt of data, brief period of time. Upon completion of the scanning operation, a trigger release signal would be loaded into the first latch and communicated from the control processor 159 to the application processor 158. Upon receipt of the signal and completion of any data processing operations remaining as a result of the receipt of data via the data bus 209, the application processor instructs the control processor to apply a "wake-up" signal to the control signal line 172 upon occurrence of any specified event requiring processing of data, after which the application processor re-enters an idle state. Thus, in accordance with the presently preferred embodiment, in the event of the direct receipt of a string of data by the application processor 158, the control processor 159 continues to control the application processor 158 in transmitting control codes to selectively enable or disable the application processor 158 to directly receive data via the data bus 209. The receipt data by the application processor 158 is referred to as "direct" data input, since the contemplated transfer of data via the data latches 186 and 193 or via the interface circuit 168 is bypassed.

FIG. 14 shows in form of a block diagram preferred electrical components of an exemplary data terminal 10, and of the preferred interactive relationship of such components to the application processor 158 or the control

processor 159. FIG. 14 shows schematically a plurality of electrical components which are generally directly related to the functional elements discussed with respect to FIG. 11. In the embodiment shown in FIG. 14, the application processor 158 controls directly the previously referred to high speed asynchronous communications interface 174 and the RS-232/485 standards serial interface 206. The flash EPROM programmable read-only memory 161 is in the embodiment of FIG. 14 identified as having a preferred 256K byte storage capacity. The flash EPROM supplements the standard ROM memory 162 which is preferred to have a 512K byte storage capacity. In the preferred example of the data terminal 10, the ROM provides the typical and normally non-variable data processing protocol instructions and includes control instructions for standard display updating routines as well as other routines which are typically implemented by standard keyboard instructions and which pertain to typical data input and output commands.

The random access memory 163 is in the specific embodiment a semi-permanent static RAM type circuit and has a preferred capacity of 512K bytes. The preferred data storage capacity has been determined to provide sufficient storage for an on-board data base related to typical inventory or delivery route type information. In view of the portability of the data terminal 10, an unexpected loss of battery power may bring about a significant loss of information unless the data stored at the time of a temporary loss of battery power are protected from destruction until full battery power is restored. For example, the data terminal 10 may be returned at an initial signal of "low battery" to a battery charger unit (not shown) for a recharging operation and any stored data may be transferred, even while the battery 177 is being recharged, from the data terminal 10 to a host computer (not shown).

A preferred LCD display 164 is a graphic display

having an array of 48 x 100 pixels. Typical menu or special graphic screen data may be pre-established for a particular data terminal 10 or for an application group of such units and may be stored initially in the specific ROM 162 provided for the particular unit or units 10. As previously discussed, the updating of displayed data on the screen device 164 requires a significant amount of data processing. Typically, such data processing operations involve accessing permanently stored screen display information, such as from the ROM 162 or from the flash EPROM 161, the manipulation of such information, and temporary storage of such manipulated information in the random access memory 163. As shown in FIG. 14, the application processor 158 has direct functional control over the respective devices for such data updating manipulations with respect to the LCD Display screen 164.

Another function related to the preferred LCD display screen 164 involves a contrast control circuit 166. The contrast of the LCD display screen 164 is typically set and adjusted by an operator and is a matter of choice. The contrast may be adjusted for example by a typical key depression or by a keyboard sequence given by an operator. Such control input executions are within the scope of operations of the control processor 159. Thus, in response to an appropriate command from the keyboard 167, the display contrast may be changed without activating the application processor 158. The contrast display may be controlled as indicated in FIG. 14 by the functional coupling of the keyboard circuit 167 to the control processor 158 and the further coupling of the processor 158 to the contrast control circuit 166 and then directly to the LCD display screen circuit 164.

The LCD display screen 164 in the preferred embodiment is equipped with a backlighting drive. Many warehouse operations, route delivery operations and even merchandising inventory operations require at least some operations of the data terminal units to be performed

under sufficiently poor lighting conditions to suggest a need for a backlighting source to be supplied as a standard feature of the LCD display screen 164. The backlight drive circuit 171 is preferably coupled through the interface circuit 168 to the control processor 159. In that such a backlighting circuit may have a need for adjusting, for example, the brightness or luminescence of the circuit, both the application processor 158 and the control processor 159 may interact through the interface circuit 168 to provide for an operator controlled brightness control sequence to be communicated to the backlight drive 171.

It should be realized that the interface circuit 168 is a simplified schematic representation of a large-scale integrated circuit 168 which includes timing function circuits for the real time clock and its functions, as well as for providing the clocking signals to each of the two processors 158 and 159. The circuit 168 further provides the already described data communication functions between the application processor 158 and the control processor 159 as represented in FIG. 11 by the two latching circuits 186 and 193. The function by the control processor 159 to activate or "wake up" the application processor for data processing operations is accentuated in the representation of the "wake-up" feature by the separate function line 172 in FIG. 14. In one contemplated embodiment the interface circuit 168 may include integrally a switching circuit function for separately switching the application processor 158 off or on, as indicated by the function blocks "#1 OFF WAIT" and "#1 ON", as shown in FIG. 15. Such a switching operation may be implemented by a typical switch as part of the integrated interface circuit 168 which selectively interrupts and reestablishes the clocking signal to the application processor 158. The function of deactivating and reactivating the application processor is controlled in a preferred embodiment via the interface circuit 168 in

a somewhat different manner. Instead of controlling the clocking circuit to the application processor 158 in the integrated circuit with a control signal from the control processor 159, the control function is preferably split. It has namely been found expedient for the application processor 158 to provide a shutdown status signal to the control processor 159 and to shut itself down. The control processor 159 subsequently returns the application processor 158 to an active state upon occurrence of any event which requires the operation of the application processor 158. The process flow diagram of FIG. 15 generally depicts operational procedures between the application processor 158 and the control processor 159.

Further in reference to FIG. 14, a trigger control signal of the scanner 210 is preferably received by the control processor 159. However the data flow from the scanner 210 will be received directly by the application processor 158 for further processing and storage. Input signals which are received at speeds within the operational envelope of the control processor 159 are received by and transferred through the control processor 159. For example, key depression signals from the keyboard 167 are preferably received directly by the control processor 159. A preferred keyboard size for the data terminal 10 referenced herein, as indicated in FIG. 14 is a 6x8 key matrix. Such a choice is made based on space considerations and requires that multiple functions may be implemented by each of the keys. However, the selection of a preferred keyboard remains in any case one of choice and has no particular bearing on the gist of the invention. Because of the "slow" realtime selection by an operator in comparison to the "fast" processing speed of even the slower control processor, the selection interpretation of which key function has been selected by an operator may be made by the control processor 159. An "event" indication character communicated to the application processor 158 preferably reflects already

which of the available functions of a particular key has been selected. The preprocessing of relatively slowly occurring events has been found to advantageously limit the operational periods of the application processor 158.

The control processor further controls an input to an audible alarm circuit 211 ("BUZZER"). An audible alarm is a slowly occurring input signal to generate a signal at audio frequency, so as to alert an operator of an alarm condition or to signal that a processing operation has been completed. For example, when the application processor 158 has received a string of data from the scanner 210, and has further processed the received information to verify its correctness, the application processor 158 may communicate an acceptance code to the control processor 159 and be shut down from further operation. The control processor will then routinely generate an audible signal to alert the operator of the unit of the acceptance of the code read via the scanner, for example. Prior to communicating the acceptance code to the control processor, the application processor may have retrieved from its memory 163, for example, information relating to the bar code which has just been read and accepted, and may have compiled an information screen displaying such retrieved information to the operator prior to the deactivation of the application processor 158. Thus, by the time the operator is alerted by the audible signal that the respective bar code has been read and accepted, the pertinent information regarding the item represented by the bar code is already displayed on the LCD display screen 164.

Other devices which are preferably under direct control of the control processor 159 are the radio 176 with its included radio interface ("RADIO INTERFACE"), and the power control circuit 178 ("CHARGE/ POWER CONTROL") of the data terminal 10. The serial interface 207 ("RS-232/RS-485 SERIAL INTERFACE") may optionally be controlled by the control processor 159. Based on the power saving

interaction between the application processor 158 and the control processor 159 various other additions of devices or functions to the general operation of the data terminal 10 may be feasible without unduly limiting the operational cycle of the data terminal 10.

The interaction between the control processor 159 and the application processor 158 is described in greater detail in reference to both FIGS. 14 and 15. In general, the operations of the application processor are restricted to data processing operations while the operations of the control processor 159 pertain to input-output control functions which include periodic monitoring functions, such as monitoring the state of the battery 177 via the charge/power control circuit 178. Though being less powerful and operating slower than the application processor 158, the control processor 159 controls the activation or reactivation of the application processor 158. However, the application processor 158 is preferred to process the parameters and feed the respective instructions to the control processor 159 by which the control processor is operated. The application processor 158 is therefore according to the preferred embodiment the one device which accesses the operations protocol of the data terminal 10 from either the ROM 162 or the flash EPROM device 161.

With the depression of the power switch by an operator, the data terminal unit is physically started with a cold start ("POWER ON"). The turn-on starts the clocking signal and the reset of both the control and application processors 158 and 159. The control processor 159 may reset the application processor 158 ("RESET #1"). The reset operation starts the apparatus ("START APPARATUS") with an initialization sequence of communications between the application processor 158 and the control processor 159. During the initialization the application processor 158 retrieves from its program storage default values, such as for a battery threshold

value and transfers the respective default value to the control processor 158 ("COMM.1"). The control processor retains the default value and uses it in its further operations to operate the power control circuit 178. Other initialization values may be communicated to set an initial contrast value on the LCD screen display 164 ("COMM.2"), and whether or not the backlighting function is to be turned ("COMM.3"), for example. The application processor 158 further may retrieve data from memory 161, 162 or 163, and manipulate such data to place an initial screen display on the screen to signal to the operator that the data terminal 10 is operational. Upon completion of data manipulation and communication of the default values for initializing the data terminal 10, the application processor 158 communicates to the control processor 159 that it is assuming its rest state ("#1 OFF WAIT") and is shut off pending the occurrence of an event.

Upon occurrence of an event, such as a "battery low indication" or the depression of a key by the operator of the data terminal 10, the control processor 159 causes the application processor 158 to become turned on ("#1 ON"). Typically the clock signal to the application processor 158 may be provided by a control signal applied to the interface circuit 168, or the application processor may become otherwise enabled, such as by an enable signal applied to the control signal line 172. Upon having become activated, the application processor 158 communicates with the control processor 159, such as via the interface circuit 168 in the manner also described with respect to FIG. 11, to request ("#1 REQU. EVENT") data as to the type of event that has occurred. After receiving the respective communication from the control processor 159, the application processor 158 tests the received information as to the type of event and proceeds to process data as required according to the program. FIG. 15 shows three typical events of a large number of programmed events for which the application processor 158

may be activated. A typical key depression may result in reading the value of the depressed key from the second data latch 193 as described with respect to FIG. 11, or from an equivalent register of the integrated circuit 168 in FIG. 14. The information then results in the retrieval of data regarding the addresses of pixels which will be changed to a logical "high" to depict the information on the LCD display screen 164, the respective data being transferred to the respective circuit elements of the display screen 164. Thereafter, the application processor communicates to the control processor 159 that the instructions have been executed and is shut down to await a further activation and "EVENT" instruction. The shutdown of the application processor 158 may be initiated either by the application processor 158 itself or by the control processor 159. Because the start-up or activation of the application processor 158 is initiated by the control processor 159, it may be desirable to disable the application processor 158 through the control processor 159.

Another typical event for activating the application processor 158 may be the detection of a low battery indication in response to a threshold value transferred by the application processor 158 to the control processor 159 during the described start-up procedure. The protocol may require that the application processor 158 verify the low battery indication by providing its own comparison check. Because of an impending shutdown due to a low battery indication, the application processor may complete any operation if the low battery indication is still within tolerable low limits or may suspend further data processing because of risk of errors in its operation due to the low battery voltage. The application processor may further display a low battery indication ("DISPLAY LOW BATT WARNING") on the LCD display screen 164 and then be shut off pending further event instruction as shown in FIG. 15.

Another type event may be a special function key instruction such as the indication that a menu operation has been selected. The application processor 158 proceeds to access a designated program routine corresponding to the requested menu choice ("RETRIEVE MENU DATA"). The respective program instructions are executed ("PROCESS DATA"), and the result or completion of the routine is displayed on the LCD display screen 164 ("DISPLAY DATA"). The displayed result may be preceded by a repetitive interactive data transfer between the application processor 158 and the control processor 159, for example, when the menu choice requires the transmission of displayed information to a host computer. In such an event the application processor 158 may transfer the displayed information character by character to the control processor 159. The control processor 159 in turn activates the radio interface and transfers the information string to the radio interface to be transmitted in accordance with the program instructions interpreted by the application processor 158. FIG. 15 shows an error trap ("ERROR") to which the program instructions proceed if an event code is not recognized by however many event descriptions and resulting processing routines by the application processor 158 may have been programmed into the application program for the particular application of the data terminal 10. It has been found that on the average, data processing operations performed by the application processor 158 require less than 10 milliseconds. Thus, on the average, operations including the processing of keystrokes and the associated display manipulations require less than one fiftieth of the average operational period of the data terminal 10. Substantial power savings are consequently achieved by selectively de-activating and re-activating the application processor for preprogrammed events which require the execution of the respective data manipulations at a speed which is not obtainable by the preferred

control processor 159.

Further in reference to FIG. 15, if none of the event tests recognize the particular code supplied for identification to the application processor 158, an event error trap routine ("ERROR") would be used to inform the operator of the error condition. Such a routine may, for example, instruct the operator to again enter the most recently requested operation, and may accompany the error routine by an audible warning from the buzzer. Various changes in the described preferred control sequence may be implemented. Certain routines may be implemented at the described slower speed by the control processor 159 directly, while the application processor 158 remains deactivated. Other changes may be made in the selection of the first and second microprocessor devices 158 and 159 as application and control processors, respectively. The described microprocessor devices have been found particularly suitable for various operations that were expected to be performed by the data terminal 10 in the above-referred to operations.

Various changes and modifications in the structure of the described embodiment are possible without departing from the spirit and scope of the invention as set forth in the claims.

CLAIMS:

1. A hand-held data collection terminal unit comprising:

a base module including a keyboard, a display, means for storing a control program and data, an interface for communicating data and a microprocessor for controlling data applied to and received from said interface in accordance with such program; and

a data and communications module including a selected one of a plurality of data communication transceivers each having unique transceiver operation signal patterns, the data and communications module further comprising a communications interface and a microprocessor communicatively coupled to the communications interface of the data and communications module and coupled to the microprocessor of the base module, the microprocessor of the data and communications module controlled to communicate data to the microprocessor of the base module in accordance with the program of the microprocessor of the base module.

2. The hand-held data collection terminal unit according to claim 1, wherein the data and communications module further comprises a data collection means having a data transfer link coupled to the microprocessor of the data and communications module for controlling the data communications between said data collection means and the base unit in accordance with the program of the microprocessor of the base module.

3. The hand-held data collection terminal unit according to claim 1, wherein the data and communications module further comprises a code reader, the code reader having a data transfer link coupled to be controlled by the microprocessor of the data and communications module for transferring data between the data and communications module and the base module in accordance with the program of the microprocessor of the base module.

4. The hand-held data collection terminal unit

according to claim 3, wherein the code reader is a CCD bar code scanner, wherein the selected communications transceiver is a radio frequency transceiver, the data and communications module having an antenna extending away from the data and communications module and the data collection terminal, the antenna being pivotally mounted to pivot away from a scanning direction of the CCD bar code scanner permitting the CCD bar code scanner to become in proximity of a bar code label to be read.

5. The hand-held data collection terminal according to claim 1, wherein the data and communications module is attached to the base module by a plurality of engaging latch hooks and corresponding latch seats and means for maintaining the engaging position.

6. A microprocessor circuit for use in data processing apparatus comprising:

means, including a first microprocessor circuit portion and signal input means for driving the first microprocessor circuit at a first clocking speed, for performing data processing operations on data signals at the first clocking speed;

means including a second microprocessor circuit portion and second timing means for driving the second microprocessor circuit portion at a second clocking speed for controlling input and output signals to and from the microprocessor control circuit;

means for communicatively coupling the first and second microprocessor circuit portions to each other to bidirectionally pass data and control signals there between; and

means for selectively deactivating the first microprocessor circuit portion upon the first microprocessor circuit portion completing a data processing operation, and for selectively reactivating the first microprocessor device in response to a control signal from the second microprocessor circuit portion, whereby the first microprocessor circuit portion remains

deactivated during periods during which no data signals are processed.

7. The microprocessor circuit according to claim 6, wherein the data processing means, the input and output controlling means and the coupling means are supported on a single circuit device.

8. The microprocessor circuit according to claim 7, wherein the single circuit device further includes the means for selectively deactivating and reactivating the first microprocessor circuit portion of the data processing means.

9. The microprocessor circuit according to claim 6, wherein the clocking speed of the first microprocessor circuit portion is at least twice that of the second microprocessor circuit portion.

10. The microprocessor circuit according to claim 6, wherein the means for communicatively coupling the first and second microprocessor circuit portions to each other comprises an interface means including a plurality of data latches, said data latches communicating with said first microprocessor circuit portion at said first clocking speed and with said second microprocessor circuit portion at said second clocking speed.

11. The microprocessor circuit according to claim 6, wherein the first microprocessor circuit portion is a 16-bit processor and the second microprocessor circuit portion is an 8-bit processor, the microprocessor circuit further comprising data storage means coupled to the 16-bit processor for at least temporarily storing data and program instructions, said data storage means including stored program instructions instructing said 16-bit processor to process data in response to the receipt of an activating control signal from the 8-bit processor.

12. The microprocessor circuit according to claim 6, wherein the first microprocessor circuit portion is a 16-bit processor and the second microprocessor circuit portion is an 8-bit processor, the second microprocessor

circuit portion further comprising storage means for controlling the operation of the 8-bit processor.

13. The microprocessor circuit according to claim 12, wherein the clocking speed of the 16-bit processor is at least twice that of the 8-bit processor.

14. The microprocessor circuit according to claim 13, wherein the 16-bit processor directly receives a string of data over a data bus from a scanning operation, while the 8-bit processor controls the access by the application processor to the data bus and further receives and transfers other periodic data to the 16-bit processor via the bidirectional communications means.

15. A microprocessor circuit for use in data processing apparatus comprising:

a first microprocessor subcircuit, including a first microprocessor block and timing means for driving the first microprocessor block at a first clocking speed;

a second microprocessor subcircuit, including a second microprocessor block and timing means for driving the second microprocessor block at a second clocking speed, the second clocking speed being functionally independent of said first clocking speed;

means for communicatively coupling the first and second microprocessor blocks to each other to bidirectionally pass data and control signals there between; and

means for selectively deactivating the first microprocessor block upon the first microprocessor block completing a data processing operation, and for selectively reactivating the first microprocessor block in response to a control signal from the second microprocessor block, whereby the first microprocessor block is coupled to operate intermittently to effect data processing operations and to become deactivated at the conclusion of the data processing operations.

16. The microprocessor circuit according to claim 15, wherein the second clocking speed is slower than the

first clocking speed.

17. The microprocessor circuit according to claim 15, wherein the first and second microprocessor blocks are discrete first and second microprocessor devices.

18. The microprocessor circuit according to claim 17, wherein the second clocking speed is slower than the first clocking speed.

19. The microprocessor circuit according to claim 18, wherein the means for communicatively coupling the first and second microprocessor devices to each other comprises an interface means including a plurality of data latches, said data latches communicating with said first microprocessor device at said first clocking speed and with said second microprocessor device at said second clocking speed.

20. The microprocessor circuit according to claim 18, wherein the first microprocessor device is a 16-bit processor and the second microprocessor device is an 8-bit processor, the microprocessor circuit further comprising data storage means for at least temporarily storing data and program instructions, the 16-bit processor being communicatively coupled to said data storage means for at least temporarily storing data and program instructions, said data storage means including stored program instructions instructing said 16-bit processor to process data in response to the receipt of an activating control signal from the 8-bit processor.

21. The microprocessor circuit according to claim 20, the microprocessor being disposed within a hand-held, portable data terminal unit including a keyboard, a display and a battery, wherein the 8-bit processor monitors the input signals from the keyboard and the display, transfers data signals received from the keyboard to the 16-bit processor for data processing operations, and receives processed data and instructional codes from the 16-bit processor in response to the transferred data signals.

22. The microprocessor circuit according to claim 21, wherein the 8-bit processor is directly coupled to a display contrast control circuit and includes means for controlling the contrast of the display of the data terminal unit.

23. The microprocessor circuit according to claim 21, wherein the 8-bit processor is coupled to a signal input terminal for receiving status input signals from a scanning module, and further comprises means for enabling the 16-bit processor to directly receive scanned data for processing in response to an input signal that the trigger of the scanning module has been activated.

24. The microprocessor circuit according to claim 21, wherein the means for communicatively coupling the 16-bit processor and the 8-bit processor to each other and the means for selectively deactivating and reactivating the 16-bit processor are formed on a single integrated circuit.

25. The microprocessor circuit according to claim 24, wherein the means for selectively deactivating and reactivating the 16-bit processor comprises means for selectively interrupting a clock signal to the 16-bit processor.

26. The hand-held data collection terminal unit according to claim 1, wherein the transceiver of the communications module is a spread spectrum transceiver, the data communications module including data modem circuit means coupled to the transceiver for communicating modulated data messages at a spread spectrum transceiver data rate bidirectionally to and from the spread spectrum transceiver, and for communicating demodulated, synchronous data messages at spread spectrum transceiver data rates to the communications interface, the communications interface comprising means for converting the synchronous data messages received from the spread spectrum transceiver to parallel data messages, and for converting parallel data messages to synchronous data

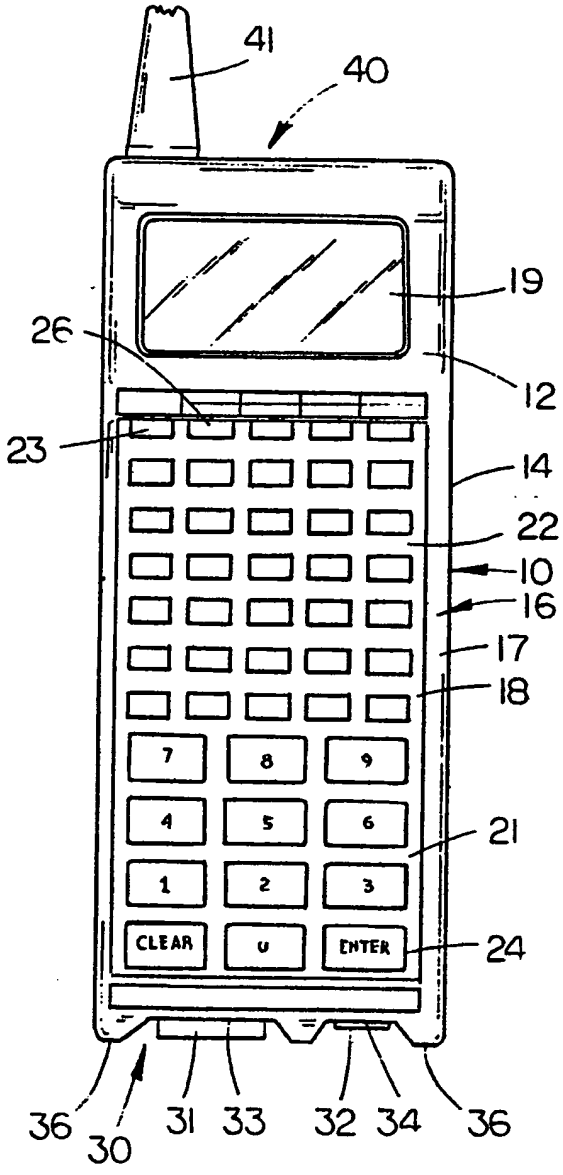
messages for communication to the modem circuit means, the microprocessor of the data communications module including means for converting the parallel data messages to serial data messages and for converting serial data messages to the parallel data messages.

27. The hand-held data collection terminal unit according to claim 26, wherein the communications module includes means for storing data messages, the data message storing means being communicatively coupled to the microprocessor of the communications module, the microprocessor of the communications module being operatively controlled to temporarily store received messages, to communicate received parallel data messages as asynchronous data messages to the microprocessor of the base module, and to communicate to the communications interface parallel data messages received as asynchronous data messages from the microprocessor of the base module.

28. The hand-held data collection terminal according to claim 26, wherein the microprocessor of the base module comprises first and second microprocessor subcircuits, the first subcircuit operable at a first clocking rate, the second microprocessor subcircuit operable at a second clocking rate which is less than the first clocking rate, the first microprocessor subcircuit being selectively operable for data processing operations and becoming deactivated upon concluding a data processing operation, the second microprocessor subcircuit monitoring and controlling operations of the base module and the communications module, and including means for selectively reactivating the operation of the first microprocessor subcircuit.

29. The hand-held data collection terminal according to claim 28, wherein the communications module includes means for storing data messages, the data message storing means being communicatively coupled to the microprocessor of the communications module, the microprocessor of the communications module being operatively controlled to

temporarily store received messages, to communicate received parallel data message as asynchronous data messages to the second microprocessor subcircuit of the base module, and to communicate to the communications interface parallel data messages received as asynchronous data messages from the second microprocessor subcircuit of the base module.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18
7
8
9
4
5
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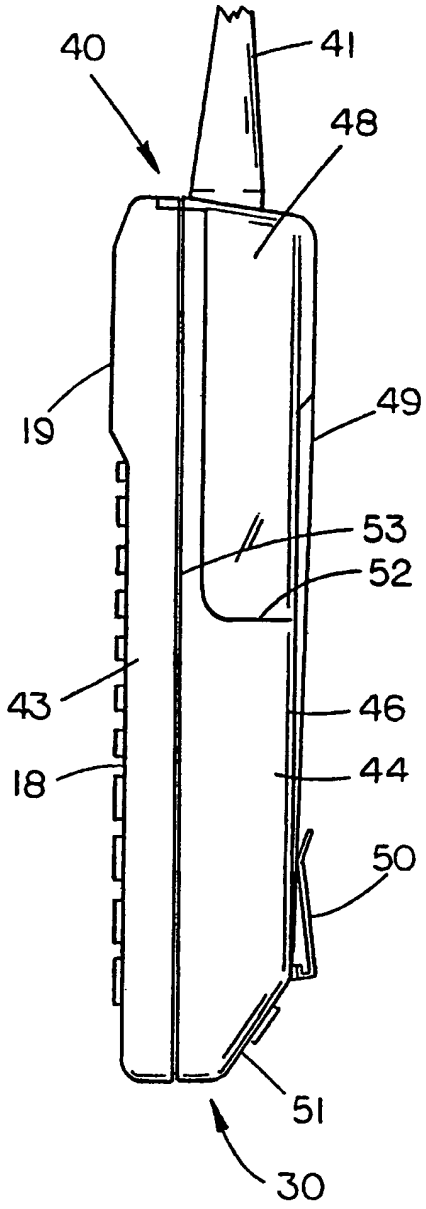
1
2
3
CLEAR
0
ENTER
24
36
30
31
33
32
34
36

FIG. 1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18
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50
51
30

FIG. 2

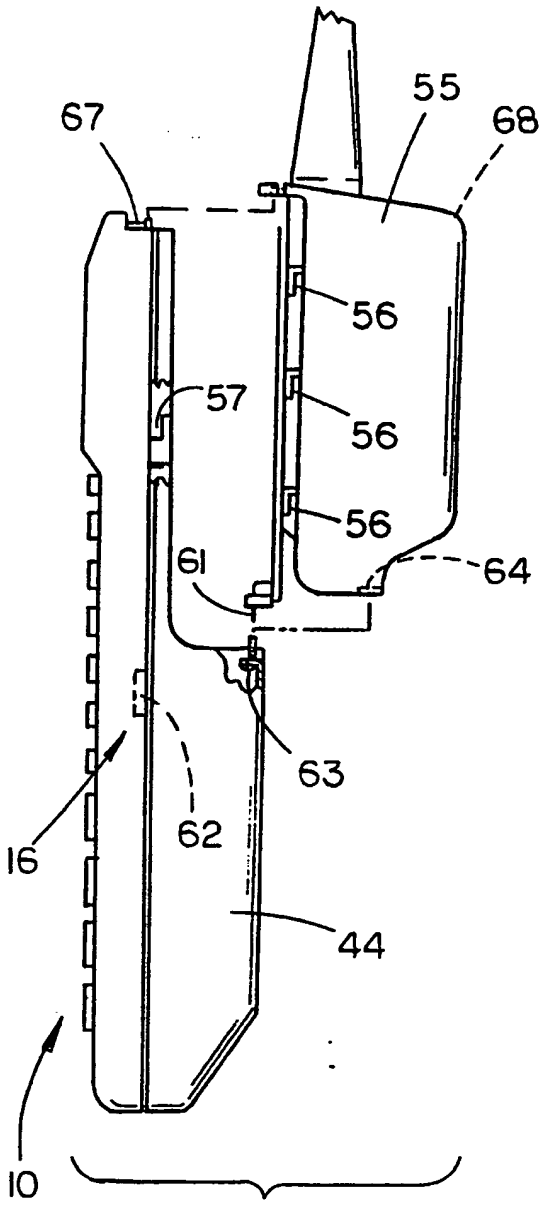


FIG. 3

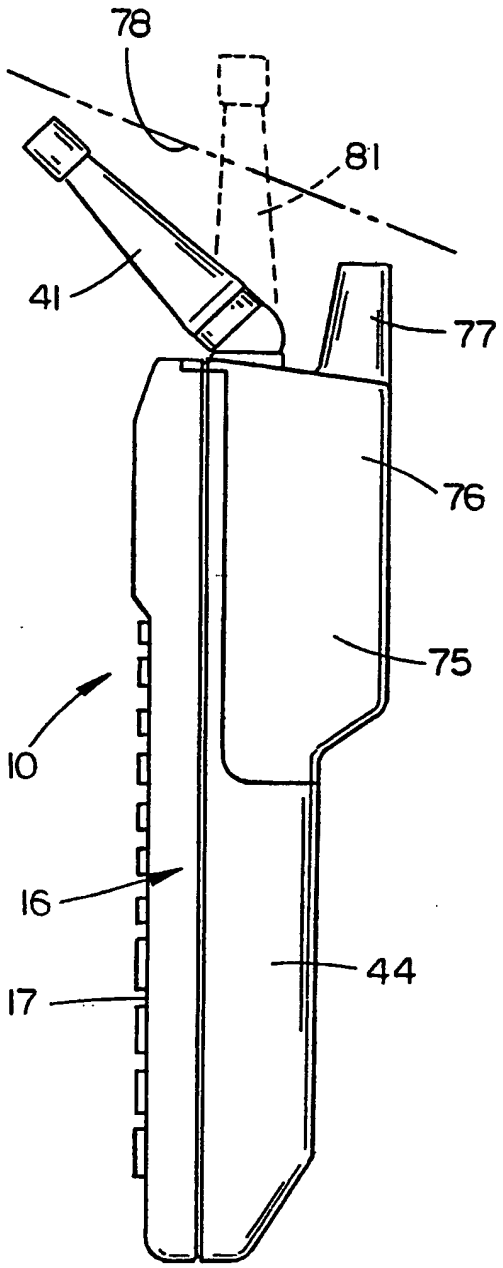


FIG. 4

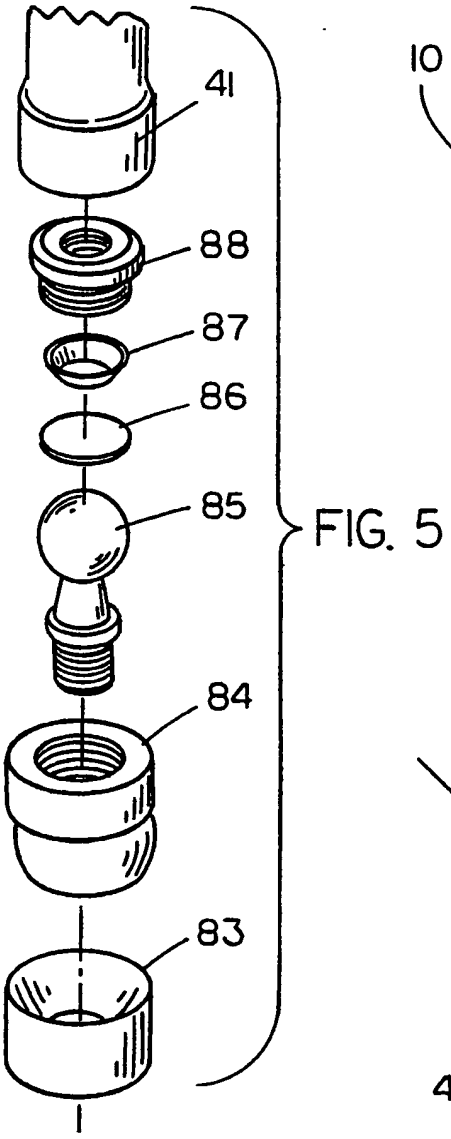


FIG. 5

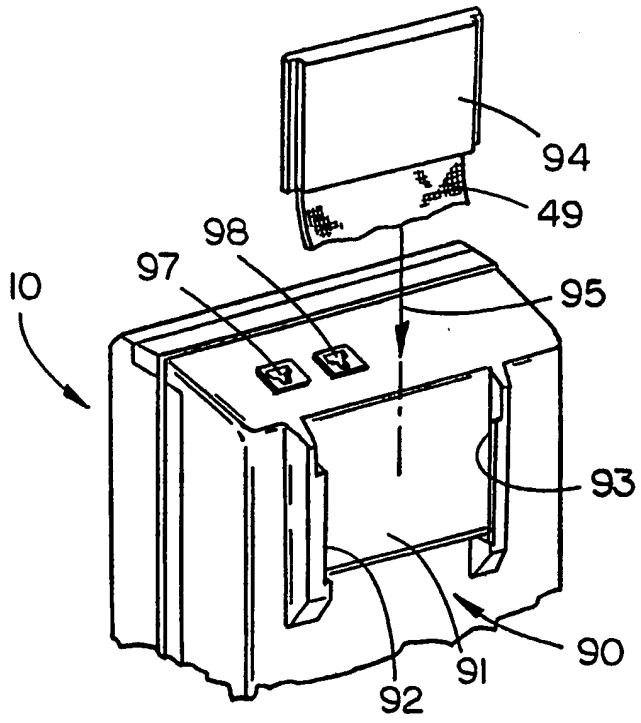


FIG. 7

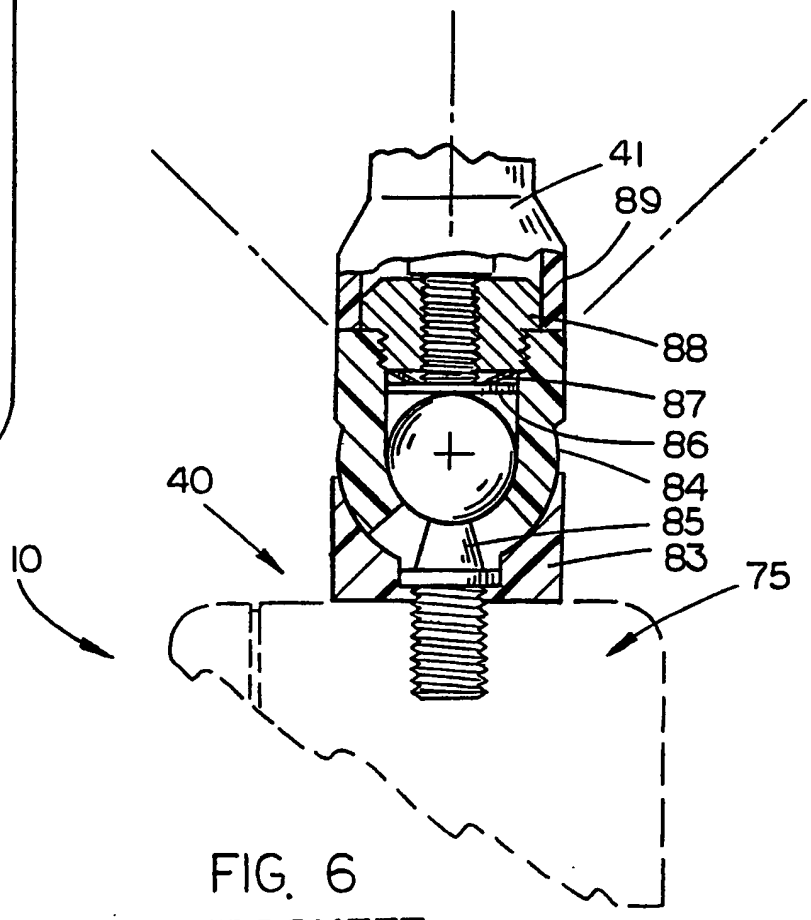
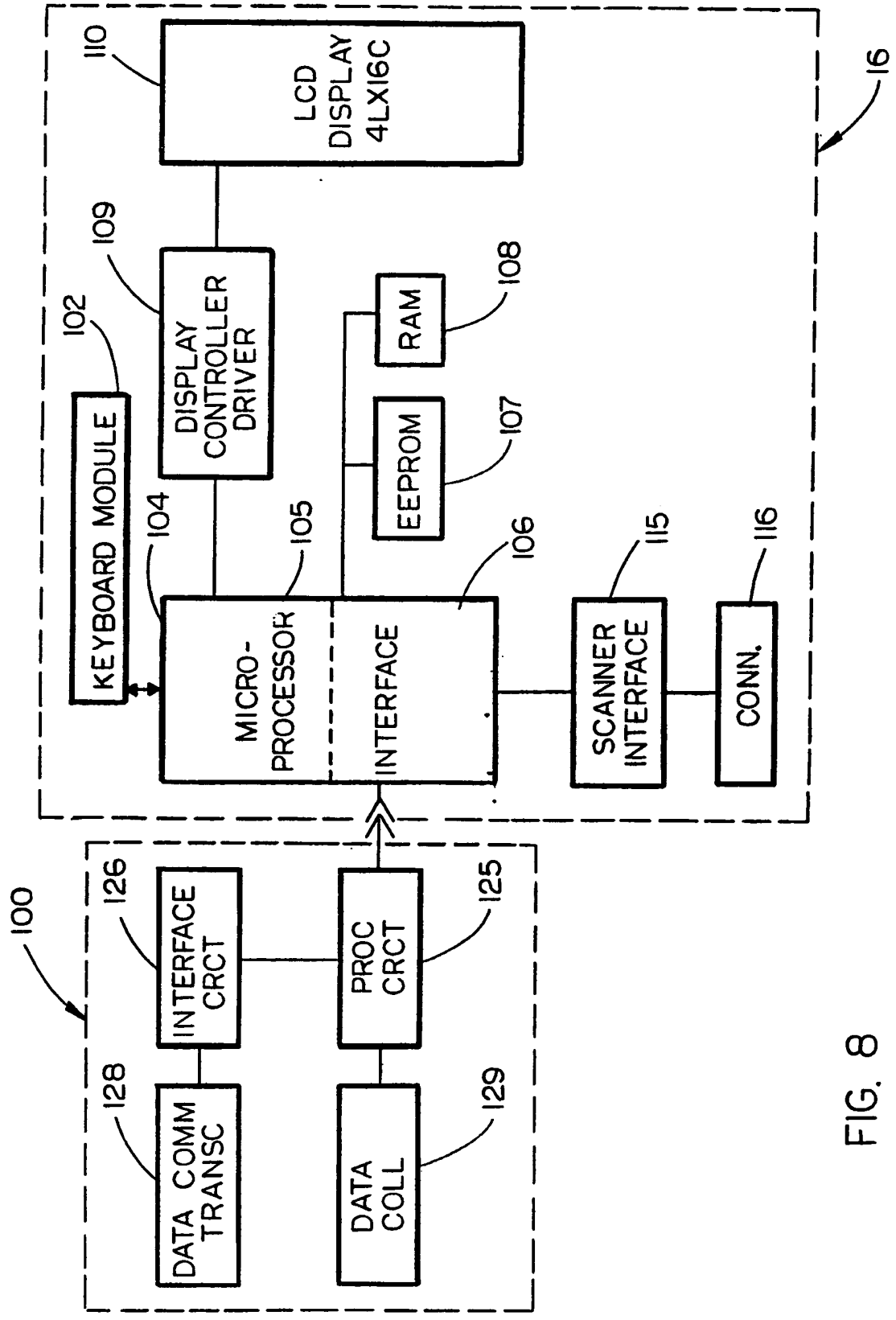


FIG. 6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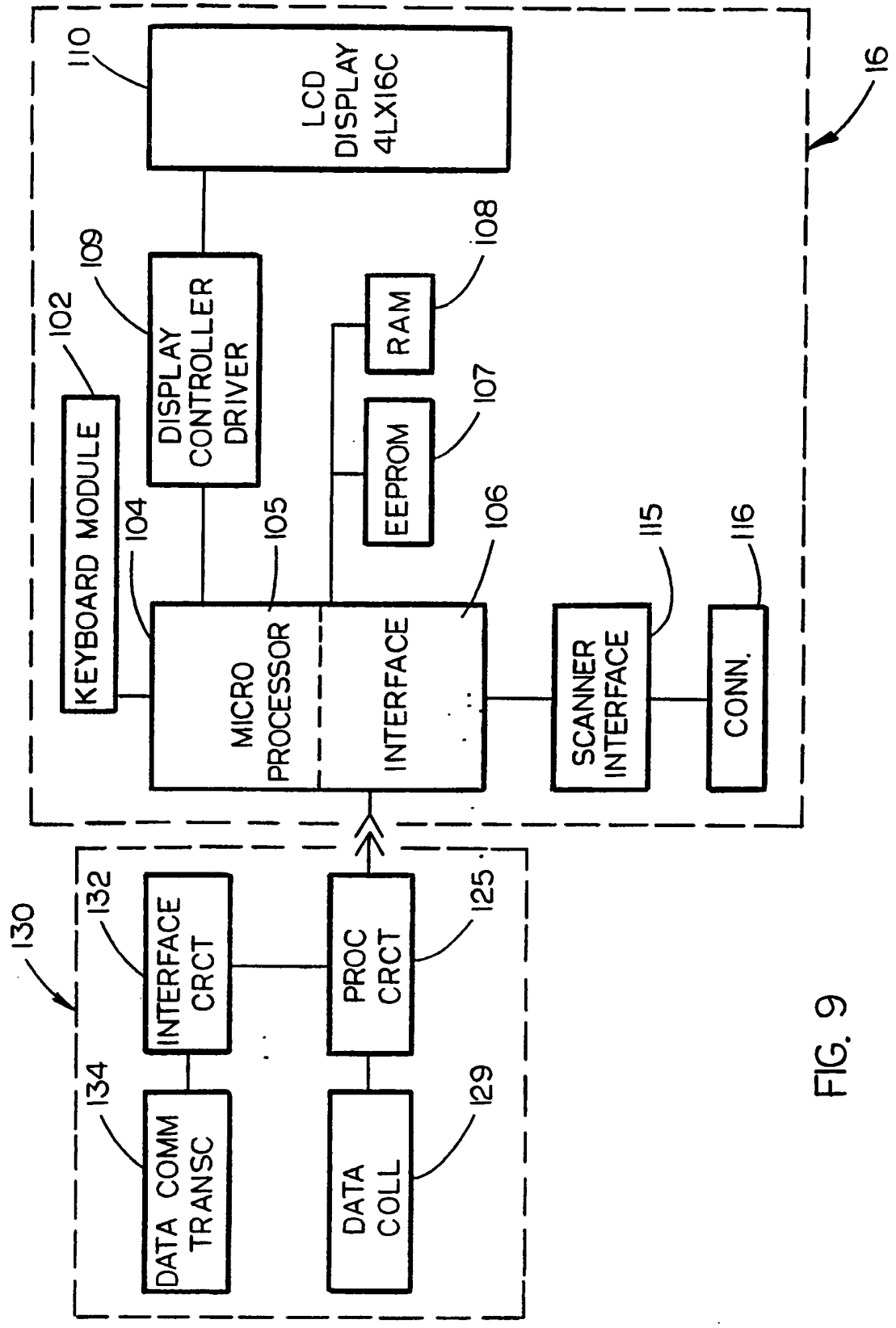
110
LCD DISPLAY 4LX16C
109
DISPLAY CONTROLLER DRIVER
102
KEYBOARD MODULE
104
105
MICRO-PROCESSOR
INTERFACE
106
RAM
108
EEPROM
107
115
SCANNER INTERFACE
116
CONN.
100
126
INTERFACE CRCT
PROC CRCT
125
128
DATA COMM TRANSC
DATA COLL
129

FIG. 8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110
LCD DISPLAY 4LX16C
109
DISPLAY CONTROLLER DRIVER
108
RAM
102
KEYBOARD MODULE
107
EEPROM
104
105
106
115
116
MICRO PROCESSOR
INTERFACE
SCANNER INTERFACE
CONN.
130
132
INTERFACE CRCT
PROC CRCT
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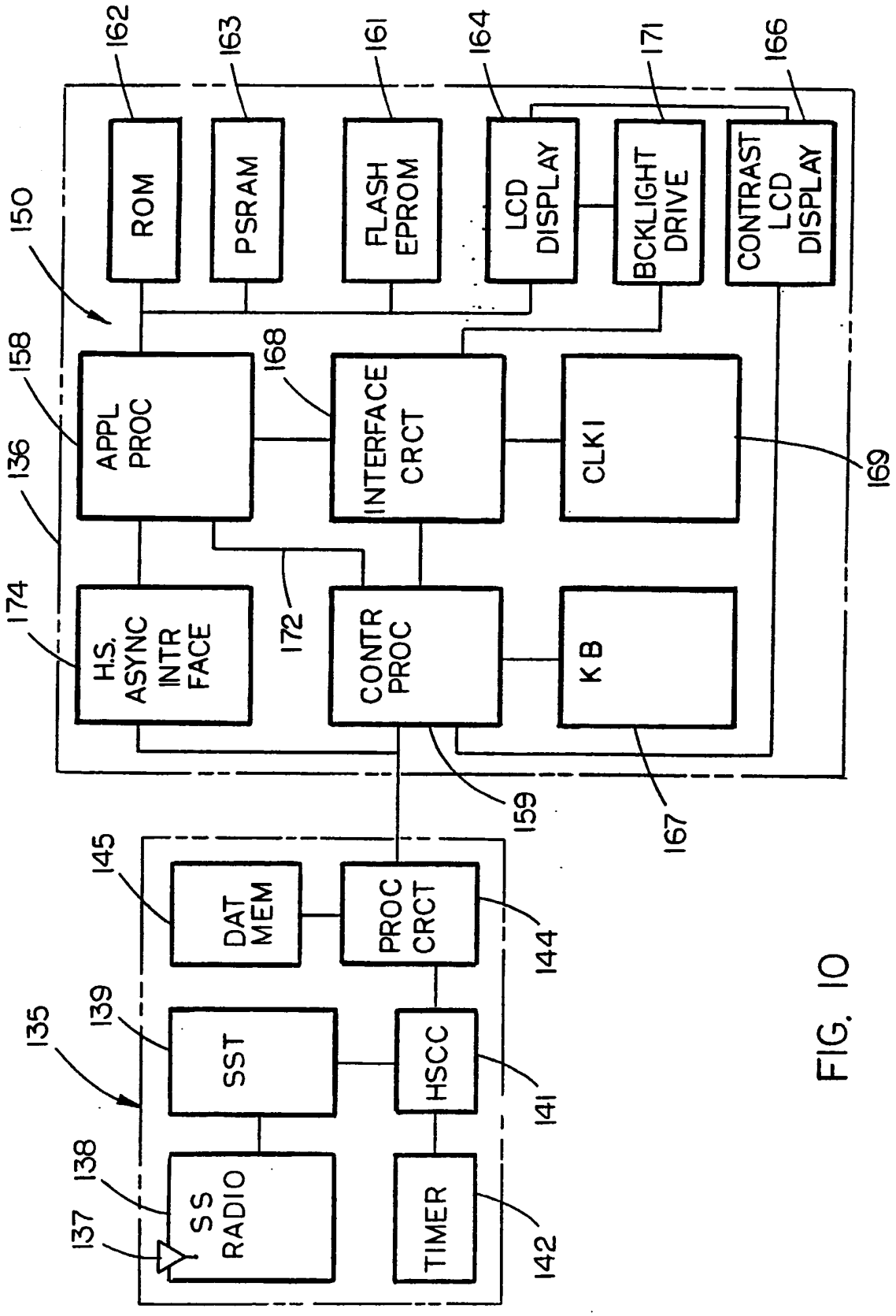
134
129
DATA COMM TRANSC
DATA COLL

FIG. 9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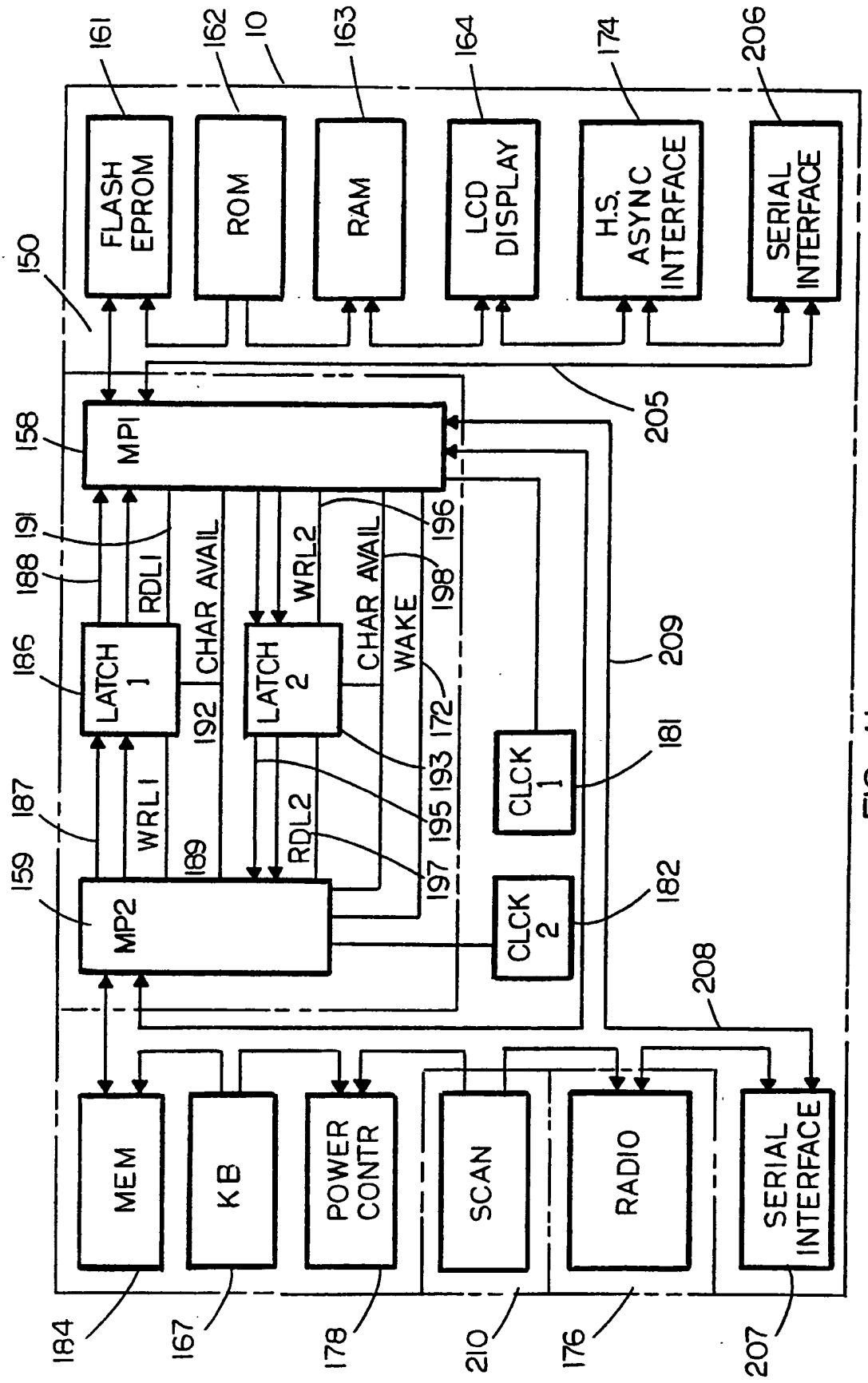
163
161
164
171
166
ROM
PSRAM
FLASH EPROM
LCD DISPLAY
BCKLIGHT DRIVE
CONTRAST LCD DISPLAY
150
158
168
APPL PROC
INTERFACE CRCT
CLK1
169
136
174
172
H.S. ASYNC INTR FACE
CONTR PROC
K B
159
167
145
DAT MEM
PROC CRCT
144
135
139
SST
HSCC
141
138
137
SS RADIO
TIMER
142

FIG. 10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162
10
163
164
174
206
FLASH EPROM
ROM
RAM
LCD DISPLAY
H.S. ASYNC INTERFACE
SERIAL INTERFACE
150
205
158
MPI
191
188
RDL1
CHAR AVAIL
WRL2
CHAR AVAIL
196
198
WAKE
186
LATCH 1
192
LATCH 2
172
209
181
CLCK 1
187
WRL1
189
RDL2
195
193
197
159
MP2
CLCK 2
182
208
MEM
KB
POWER CONTR
SCAN
RADIO
SERIAL INTERFACE
184
167
178
210
176
207

FIG. 11

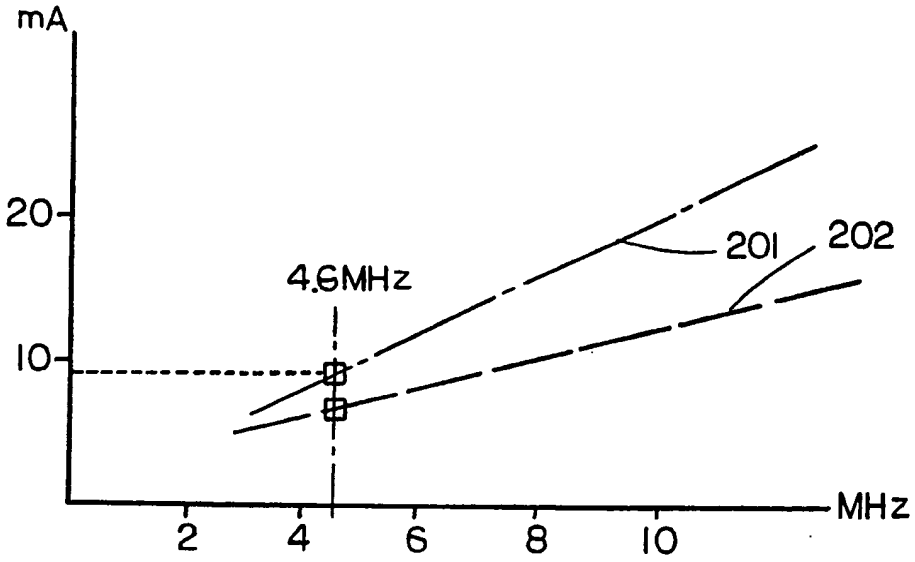
mA
20
10
4.6MHz
201
202
MHz
2
4
6
8
10

FIG. 12

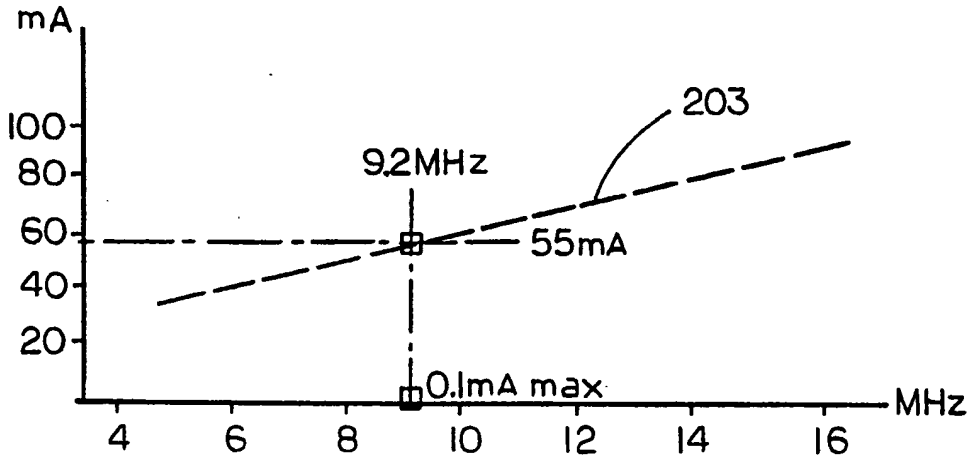
mA
100
80
60
40
20
9.2MHz
203
55mA
0.1mA max
MHz
4
6
8
10
12
14
16

FIG. 13

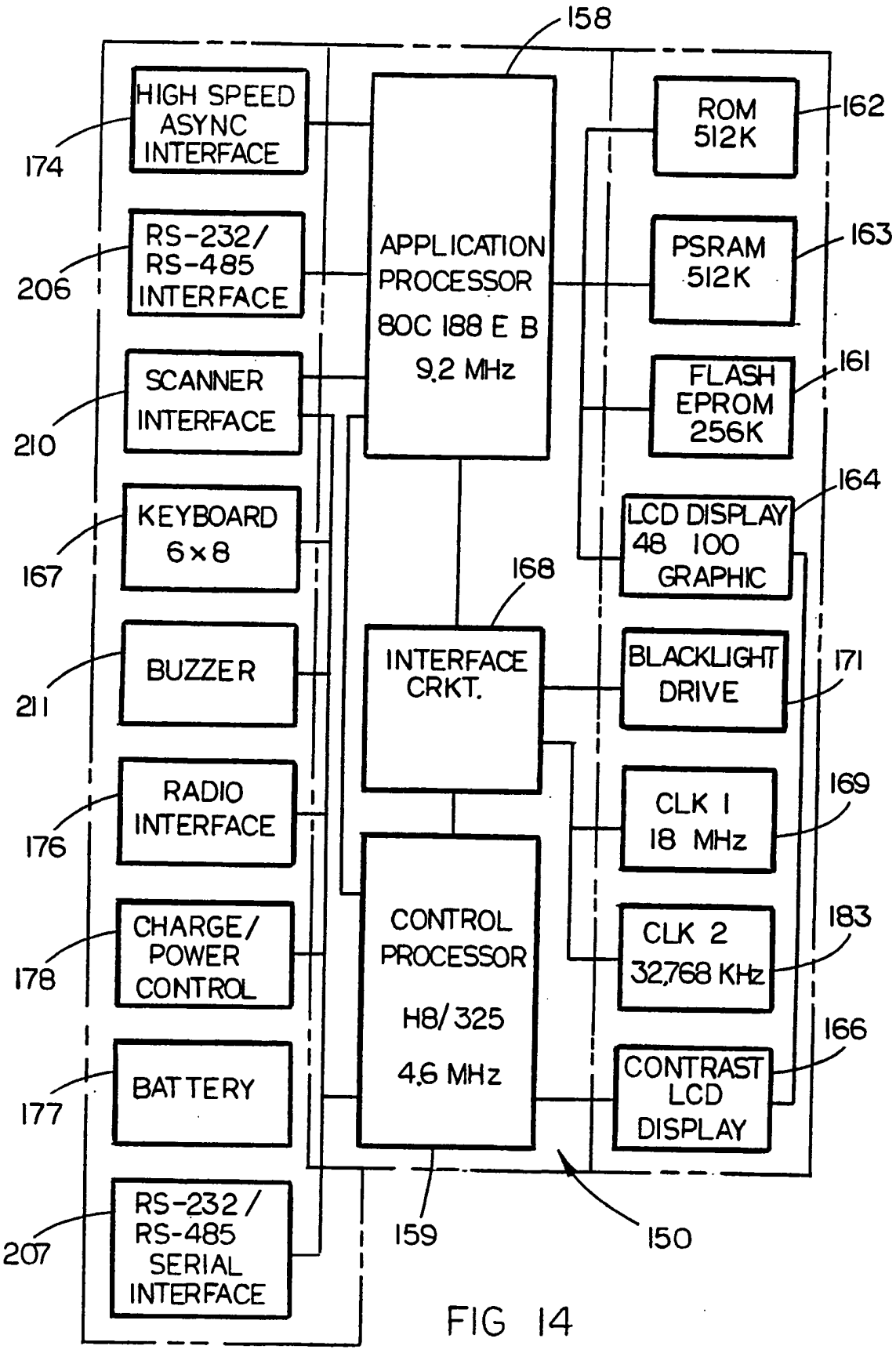
158
HIGH SPEED ASYNC INTERFACE
174
RS-232/ RS-485 INTERFACE
206
SCANNER INTERFACE
210
KEYBOARD 6×8
167
BUZZER
211
RADIO INTERFACE
176
CHARGE/ POWER CONTROL
178
BATTERY
177
RS-232/ RS-485 SERIAL INTERFACE
207
APPLICATION PROCESSOR 80C 188 E B 9.2 MHz
INTERFACE CRKT.
168
CONTROL PROCESSOR H8/325 4.6 MHz
159
150
ROM 512K
162
PSRAM 512K
163
FLASH EPROM 256K
161
LCD DISPLAY 48 100 GRAPHIC
164
BLACKLIGHT DRIVE
171
CLK 1 18 MHz
169
CLK 2 32,768 KHz
183
CONTRAST LCD DISPLAY
166

FIG 14

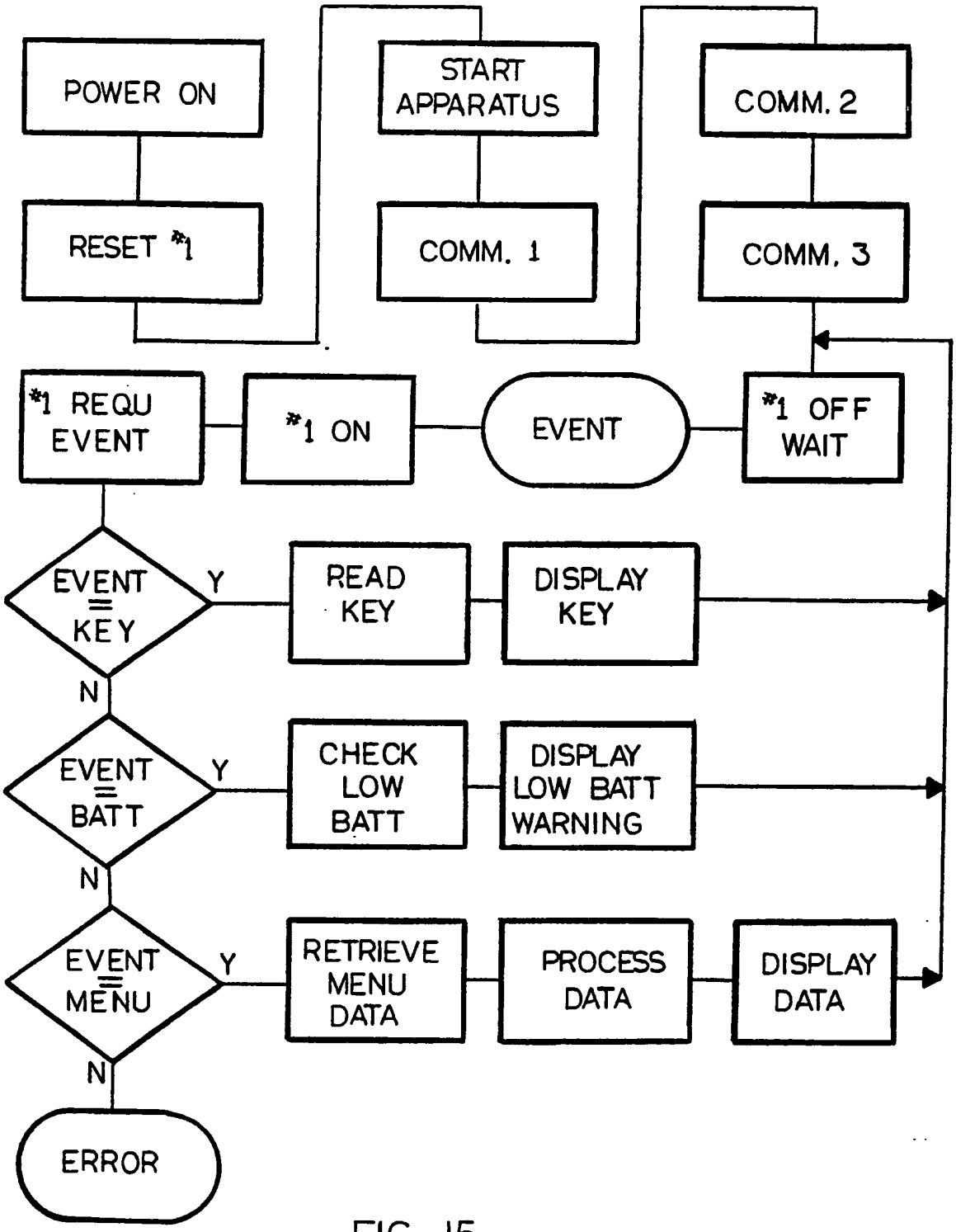
POWER ON
START APPARATUS
COMM. 2
RESET *1
COMM. 1
COMM. 3
*1 REQU EVENT
*1 ON
EVENT
*1 OFF WAIT
EVENT = KEY
Y
READ KEY
DISPLAY KEY
N
EVENT = BATT
Y
CHECK LOW BATT
DISPLAY LOW BATT WARNING
N
EVENT = MENU
Y
RETRIEVE MENU DATA
PROCESS DATA
DISPLAY DATA
N
ERROR

FIG. 15

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US92/01461

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5): -G06K 7/10 G06F 15/24

U.S.Cl.: 235/385,454,472

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S.	235/385,454,472

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	US, A, 4,471,218 (CULP) 11 September 1984 See the entire document.	1-29
Y	US, A, 4,621,189 (KUMAR) 04 November 1986 See the entire document.	1-29
Y	US, A, 4,983,318 (KNOWLES) 08 February 1991 See the entire document.	1-29
Y,P	US, A, 5,047,614 (BIANCO) 10 September 1991 See the entire document.	1-29

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
05 May 1992	16 JUN 1992
International Searching Authority	**Signature of Authorized Officer**
ISA/US	Harold Pitts

Form PCT/ISA/210 (second sheet) (Rev.11-87)